40-μA, 1.27-MHz, Micro-Power Rail-to-Rail I/O Op Amps

Features

- Stable 1.27 MHz GBWP with Low IQ of Only 40 μA Typical per Amplifier
- 0.9 V/μs Slew Rate
- Offset Voltage: 3.5 mV Maximum
- Offset Voltage Temperature Drift: 0.6 μV/°C
- Input Bias Current: 1 pA Typical
- Beyond the Rails Input Common-Mode Range
- Outputs Swing to within 5 mV Typical of each Rail
- No Phase Reversal for Overdriven Inputs
- Single +2.1 V to +6.0 V Supply Voltage Range
- −40°C to 125°C Operation Range

Applications

- Active Filters, ASIC Input or Output Amplifier
- Sensor Interface
- Smoke/Gas/Environment Sensors
- Portable Instruments and Mobile Device
- Audio Output
- Battery or Solar Powered Systems
- Medical Equipment
- Piezo Electrical Transducer Amplifier

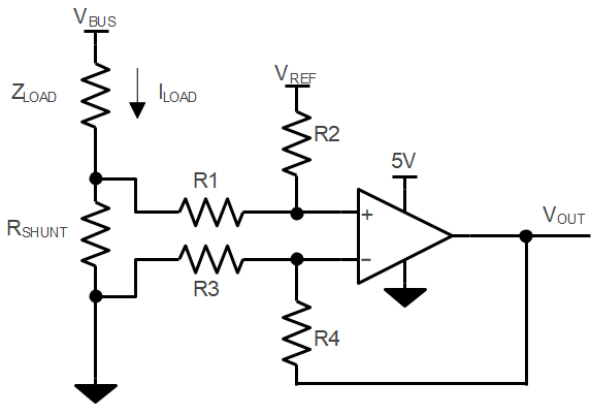
Description

LMV321TP/358TP/324TP are CMOS single, dual, and quad op-amps with low offset, stable high-frequency response, low power, low supply voltage, and rail-to-rail inputs and outputs. They incorporate 3PEAK's proprietary and patented design techniques to achieve best in-class performance e among all micro-power CMOS amplifiers.

The LMV321TP/358TP/324TP is unity-gain stable under Any Capacitive Load with 1.27 MHz gain-bandwidth product, 0.9 V/μs slew rate while consuming only 40 μA of supply current per amplifier. Beyond the rails input and rail-to-rail output characteristics allow the full power-supply voltage to be used for signal range.

This combination of features makes the LMV321TP /358TP/324TP superior among rail-to-rail input /output CMOS op-amps in its power class. The LMV321TP/358TP/324TP family is an ideal choice for battery-powered applications because they minimize errors due to power supply voltage variations over the lifetime of the battery and maintain high CMRR even for a rail-to-rail input op-amp.

Typical Application Circuit



$V_{OUT} = (I_{LOAD} \times R_{SHUNT}) \times (R2 / R1) + V_{REF}$

When R3 = R1, R2 = R4, $R_{SHUNT} << R1$

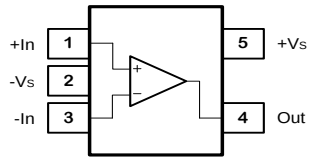
Table of Contents

Revision History

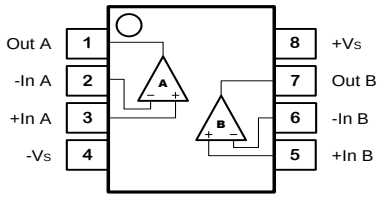
Date	Revision	Notes
2022-03-03	Rev.A.3	Updated with new document format.
2023-08-24	Rev.A.4	The following updates are all about the new datasheet formats or typo, the actual product remains unchanged. Updated to new format of package dimensions. Updated tape and reel information.

Pin Configuration and Functions

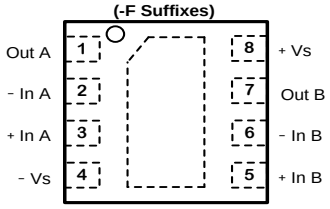
LMV321TP
5-Pin SOT23/SC70
(-T and -C Suffixes)



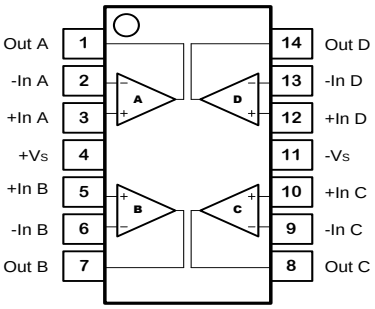
LMV358TP
8-Pin SOIC/MSOP
(-S and -V Suffixes)



LMV358TP
8-Pin DFN
(-F Suffixes)



LMV324TP
14-Pin SOIC/TSSOP
(-S and -T Suffixes)



The exposed thermal pad of DFN package should be left floated.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Supply Voltage: $V^+ - V^-$			6.0	V
Input Voltage		$V^- - 0.2$	$V^+ + 0.2$	V
Input Current: +IN, −IN, SHDN (2)		−10	10	mA
Output Short-Circuit Duration (3)			Indefinite	
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500 mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	8	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
5-Pin SC70	400		°C/W
5-Pin SOT23	250	81	°C/W
8-Pin SOIC	158	43	°C/W
8-Pin TSSOP	191	44	°C/W
8-Pin MSOP	210	45	°C/W
8-Pin DFN 2*2	100	60	°C/W
14-Pin SOIC	120	36	°C/W
14-Pin TSSOP	180	35	°C/W

Electrical Characteristics

V_{SUPPLY} = 5 V, V_{CM} = V_{OUT} = V_{SUPPLY}/2, R_L = 100 kΩ, C_L =100 pF, the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = +27°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OS}	Input Offset Voltage	V_{CM} = V_{SUPPLY}/2	−3.5	±0.1	+3.5	mV
V_{OS} TC	Input Offset Voltage Drift	T_A = +27°C		0.6		μV/°C
I_B	Input Bias Current	T_A = +27°C		1.0		pA
I_{OS}	Input Offset Current	T_A = +27°C		1.0		pA
V_n	Input Voltage Noise	f = 0.1 Hz to 10 Hz, T_A = +27°C		5.6		μV_{P-P}
e_n	Input Voltage Noise Density	f = 1 kHz, T_A = +27°C		39		nV/√Hz
		f = 10 kHZ, T_A = +27°C		23		
R_{IN}	Input Resistance	T_A = +27°C	>100			GΩ
C_{IN}	Input Capacitance	Differential, T_A = +27°C		1.5		pF
		Common Mode, T_A = +27°C		3.0		
CMRR	Common Mode Rejection Ratio	V_{CM} = 0.1 V to 4.9 V	80	110		dB
V_{CM}	Common-mode Input Voltage Range		−0.1		5.1	V
PSRR	Power Supply Rejection Ratio		80	102		dB
A_{VOL}	Open-Loop Large Signal Gain	V_{OUT} = 2.5 V, R_{LOAD} = 100 kΩ	80	102		dB
		V_{OUT} = 0.1 V to 4.9 V, R_{LOAD} = 100 kΩ	72	102		
V_{OL}	Output Swing from Supply Rail	R_{LOAD} = 100 kΩ, T_A = +27°C		5		mV
I_{SC}	Output Short-Circuit Current	Sink or source current, T_A = +27°C		45		mA
I_Q	Quiescent Current per Amplifier			40	51	μA
PM	Phase Margin	R_{LOAD} = 100 kΩ, C_{LOAD} = 100 pF, T_A = +27°C		66		°
GM	Gain Margin	R_{LOAD} = 100 kΩ, C_{LOAD} = 100 pF, T_A = +27°C		15		dB
GBWP	Gain-Bandwidth Product	f = 1 kHz, T_A = +27°C		1.27		MHz
t_S	Settling Time, 1.5 V to 3.5 V, Unity Gain	0.1%, T_A = +27°C		2.3		μs
		0.01%, T_A = +27°C		2.8		
	Settling Time, 2.45 V to 2.55 V, Unity Gain	0.1%, T_A = +27°C		0.33		
		0.01%, T_A = +27°C		0.38		
SR	Slew Rate	A_V = 1, V_{OUT} = 1.5 V to 3.5 V, C_{LOAD} = 100 pF, R_{LOAD} = 100 kΩ, T_A = +27°C		0.9		V/μs
FPBW	Full Power Bandwidth	$2V_{P-P}$, T_A = +27°C		140		kHZ
THD+N	Total Harmonic Distortion and Noise	f = 1 kHz, A_V = 1, R_L = 100 kΩ, V_{OUT} = $2V_{PP}$, T_A = +27°C		−105		dB
		f = 10 kHz, A_V = 1, R_L = 100 kΩ, V_{OUT} = $2V_{PP}$, T_A = +27°C		−90		

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500 mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.
(4) Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.
(5) Full power bandwidth is calculated from the slew rate FPBW = $SR/\pi \bullet V_{P-P}$.

Typical Performance Characteristics

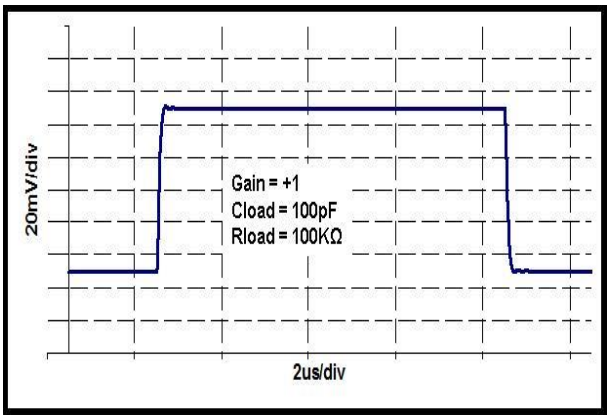


Figure 1 Small-Signal Step Response, 100 mV

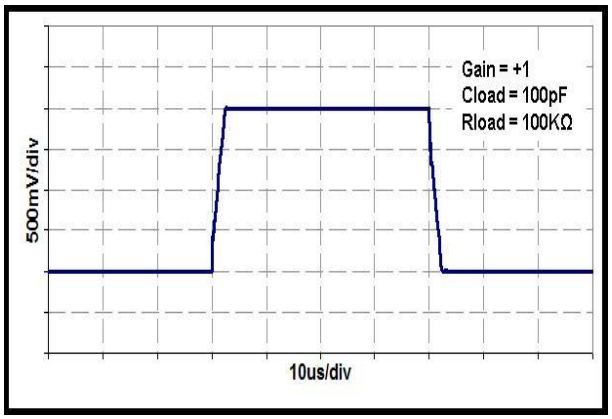


Figure 2 Large-Signal Step Response, 2 V Step

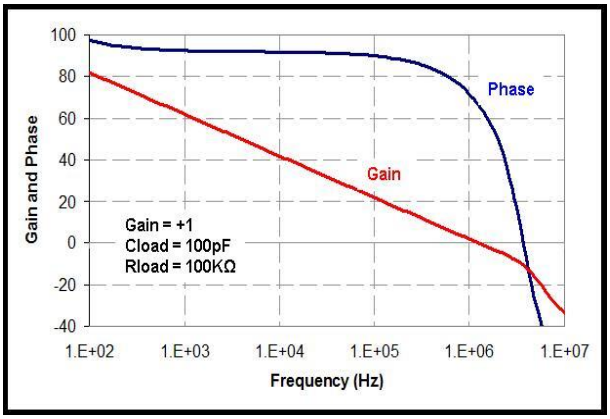


Figure 3 Open-Loop Gain and Phase

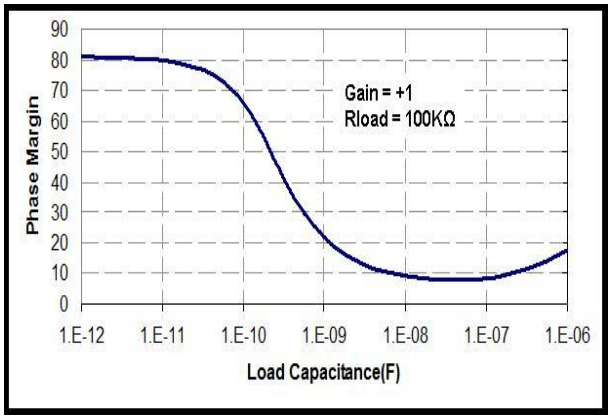


Figure 4 Phase Margin vs. C_{LOAD} (Stable for Any C_{LOAD})

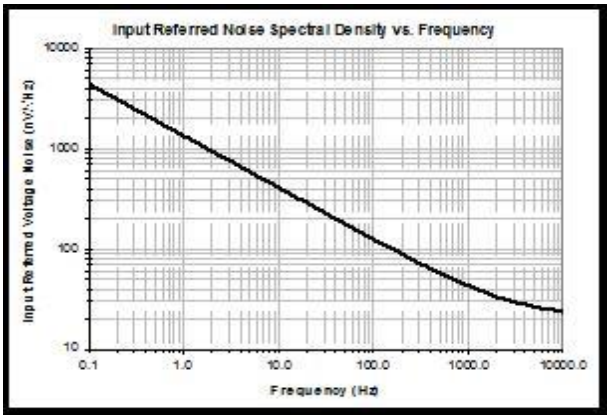


Figure 5 Input Voltage Noise Spectral Density

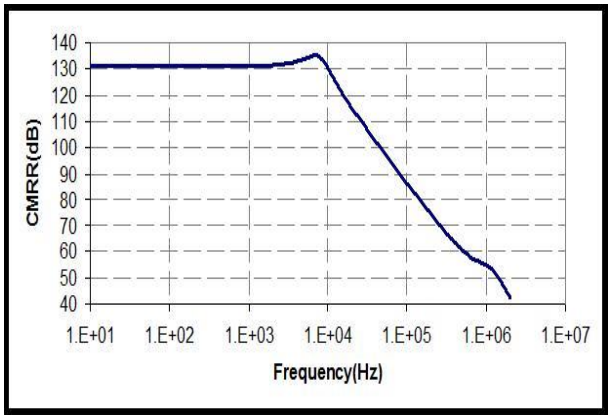


Figure 6 Common-Mode Rejection Ratio

Typical Performance Characteristics (Continued)

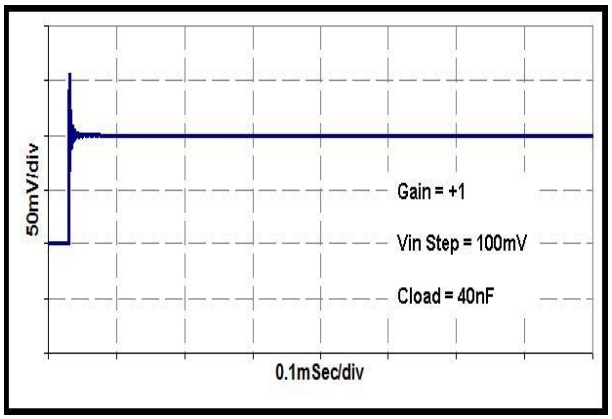


Figure 7 Over-Shoot Voltage
C_{LOAD} = 40 nF, Gain = +1

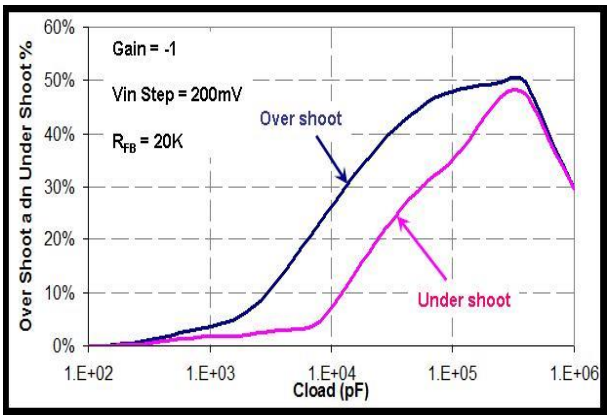


Figure 8 Over-Shoot % vs. C_{LOAD}
Gain = −1, RFB = 20 kΩ

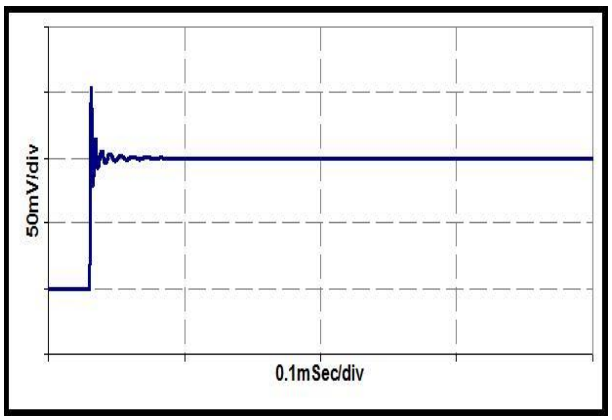


Figure 9 Over-Shoot Voltage
C_{LOAD} = 40 nF, Gain = −1, RFB = 100 kΩ

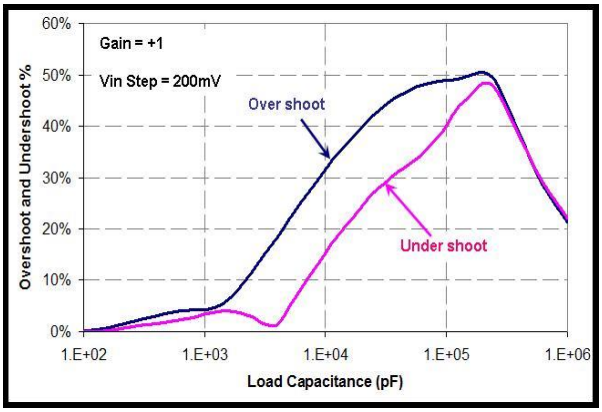


Figure 10 Small-Signal Over-Shoot % vs. C_{LOAD}
Gain = +1

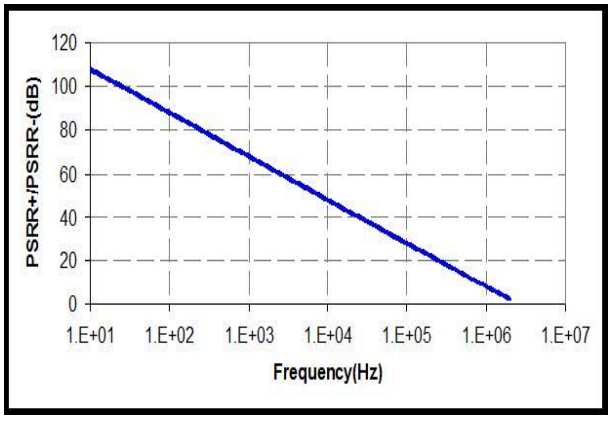


Figure 11 Power-Supply Rejection Ratio

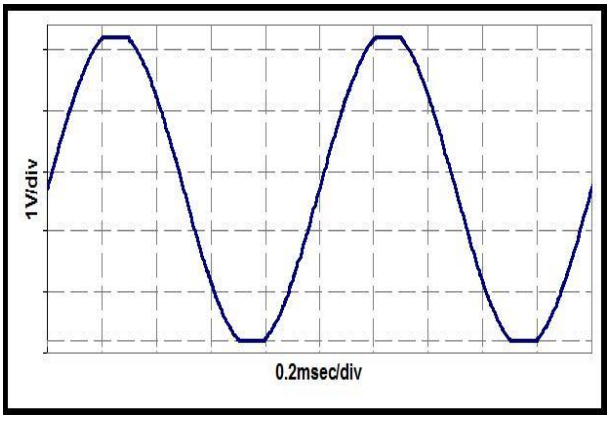


Figure 12 V_{IN} = −0.2 V to 5.7 V, No Phase Reversal

Typical Performance Characteristics (Continued)

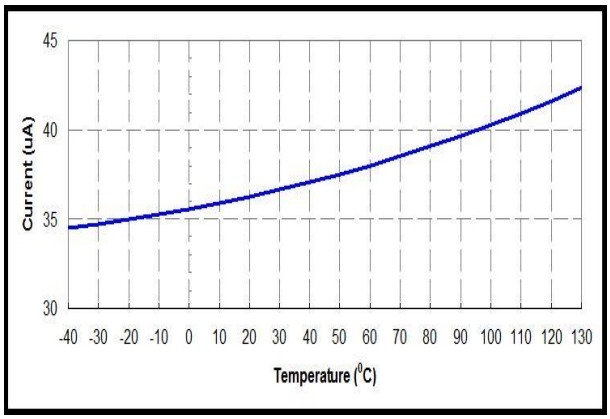


Figure 13 Quiescent Supply Current vs. Temperature

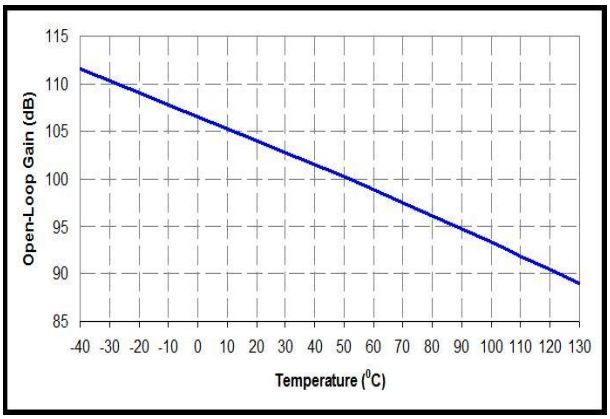


Figure 14 Open-Loop Gain vs. Temperature

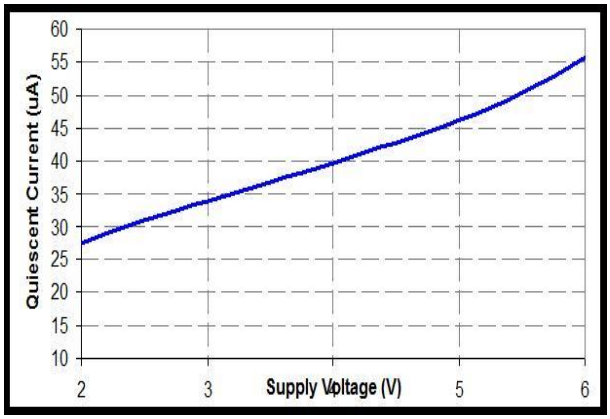


Figure 15 Quiescent Supply Current vs. Supply Voltage

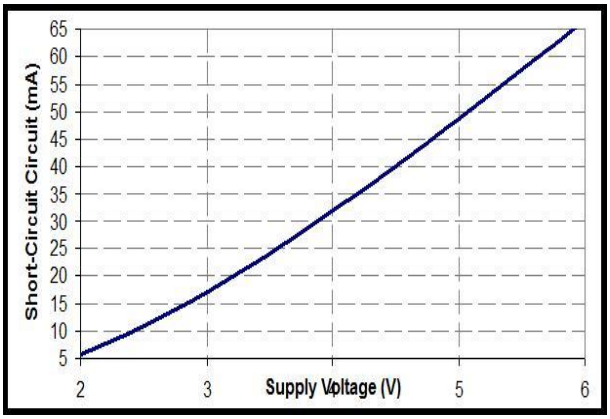


Figure 16 Short-Circuit Current vs. Supply Voltage

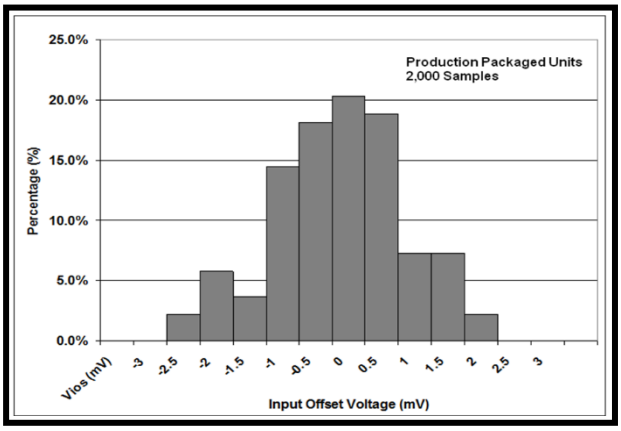


Figure 17 Input Offset Voltage Distribution

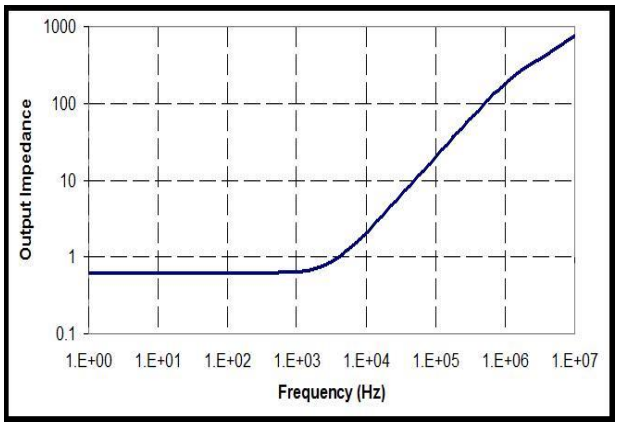


Figure 18 Closed-Loop Output Impedance vs. Frequency

Typical Performance Characteristics (Continued)

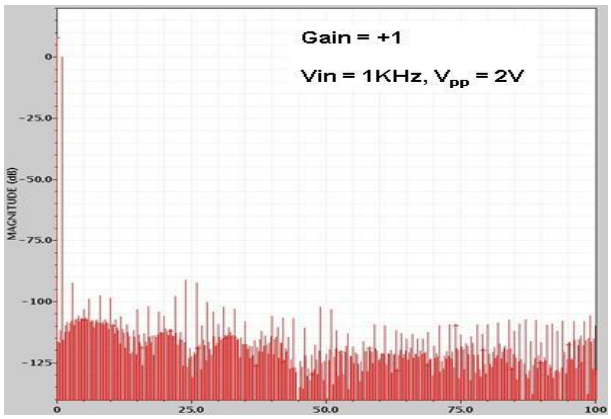


Figure 19 THD + Noise

Gain = +1, V_{IN} = 1 kHz, V_{PP} = 2 V

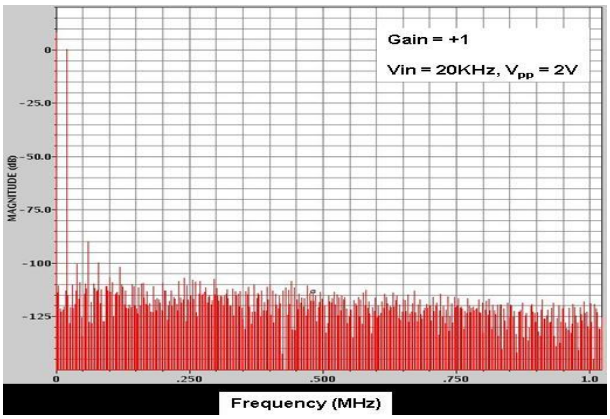


Figure 20 THD + Noise

Gain = +1, V_{IN} = 20 kHz, V_{PP} = 2 V

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Low Input Bias Current

The LMV321TP/358TP/324TP is a CMOS OPA family and features very low input bias current in pA range. The low input bias current allows the amplifiers to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on "PCB Surface Leakage" for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is 1012 Ω. A 5 V difference would cause 5 pA of current to flow, which is greater than the LMV321TP/358TP/324TP OPA's input bias current at +27°C (±1 pA, typical). It is recommended to use multi-layer PCB layout and route the OPA's −IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 21 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:

a) Connect the non-inverting pin (V_{IN+}) to the input with a wire that does not touch the PCB surface.

b) Connect the guard ring to the inverting input pin (V_{IN-}). This biases the guard ring to the Common Mode input voltage.

2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):

a) Connect the guard ring to the non-inverting input pin (V_{IN+}). This biases the guard ring to the same reference voltage as the op-amp (e.g., $V_{DD}/2$ or ground).

b) Connect the inverting pin (V_{IN-}) to the input with a wire that does not touch the PCB surface.

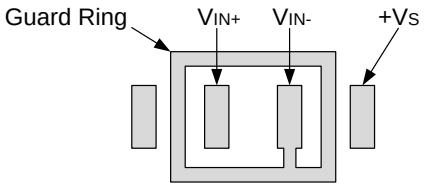


Figure 21

Ground Sensing and Rail to Rail Output

The LMV321TP/358TP/324TP has excellent output drive capability, delivering over 10 mA of output drive current. The output stage is a rail-to-rail topology that is capable of swinging to within 5 mV of either rail. Since the inputs can go 100 mV beyond either rail, the op-amp can easily perform 'True Ground Sensing'.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5 V beyond either supply, otherwise current will flow through these diodes.

Feedback Components and Suppression of Ringing

Care should be taken to ensure that the pole formed by the feedback resistors and the parasitic capacitance at the inverting input does not degrade stability. For example, in a gain of +2 configuration with gain and feedback resistors of 10 k, a poorly designed circuit board layout with parasitic capacitance of 5 pF (part +PC board) at the amplifier's inverting input will cause the amplifier to ring due to a pole formed at 3.2 MHz. An additional capacitor of 5 pF across the feedback resistor as shown in Figure 22 will eliminate any ringing.

Careful layout is extremely important because low power signal conditioning applications demand high-impedance circuits. The layout should also minimize stray capacitance at the OPA's inputs. However some stray capacitance may be unavoidable and it may be necessary to add a 2 pF to 10 pF capacitor across the feedback resistor. Select the smallest capacitor value that ensures stability.

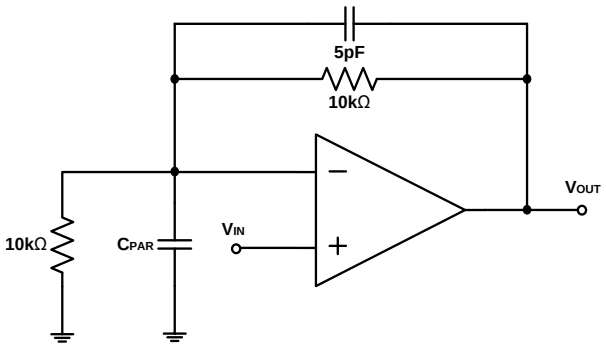


Figure 22

Driving Large Capacitive Load

The LMV321TP/358TP/324TP of OPA is designed to drive large capacitive loads. Refer to Typical Performance Characteristics for "Phase Margin vs. Load Capacitance". As always, larger load capacitance decreases overall phase margin in a feedback system where internal frequency compensation is utilized. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in output step response. The unity-gain buffer (G = +1 V/V) is the most sensitive to large capacitive loads.

When driving large capacitive loads with the LMV321TP/358TP/324TP (e.g., > 200 pF when G = +1 V/V), a small series resistor at the output (R_{ISO} in Figure 23) improves the feedback loop's phase margin and stability by making the output load resistive at higher frequencies.

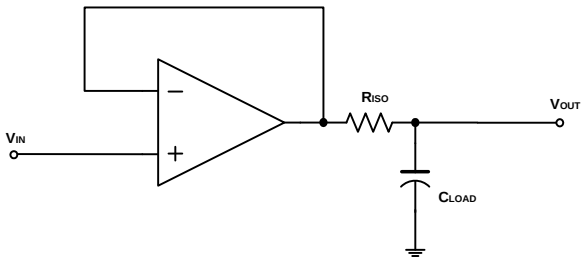


Figure 23

Power Supply Layout and Bypass

The LMV321TP/358TP/324TP OPA's power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 μF to 0.1 μF) within 2 mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1 μF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA's inputs and outputs. To decrease stray capacitance, minimize PC board lengths and resistor leads, and place external components as close to the op amps' pins as possible.

Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

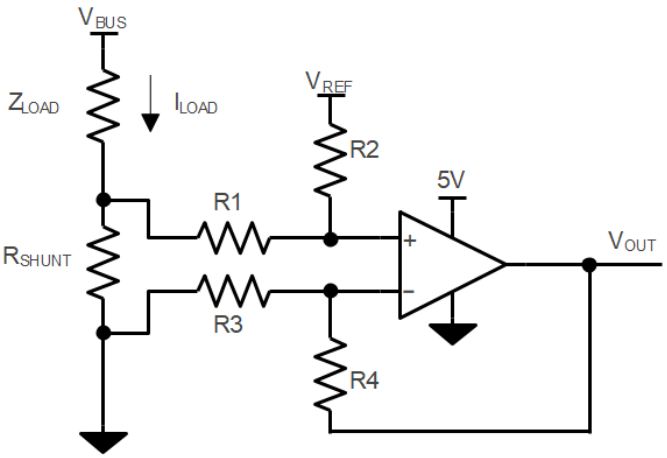
A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

Typical Application

Low Side Current Sensing Application

Figure 24 shows the amplifier configured in a low-side current sensing application. The low-side current sensing method consists of placing a sense resistor between the load and the circuit ground. The voltage dropping across the resistor is amplified by different amplifier circuits. The V_{REF} can be used to add bias voltage to output voltage. Particular attention must be paid to the matching and precision of R1, R2, R3, and R4, to maximize the accuracy of the measurement.



$V_{OUT} = (I_{LOAD} \times R_{SHUNT}) \times (R2 / R1) + V_{REF}$

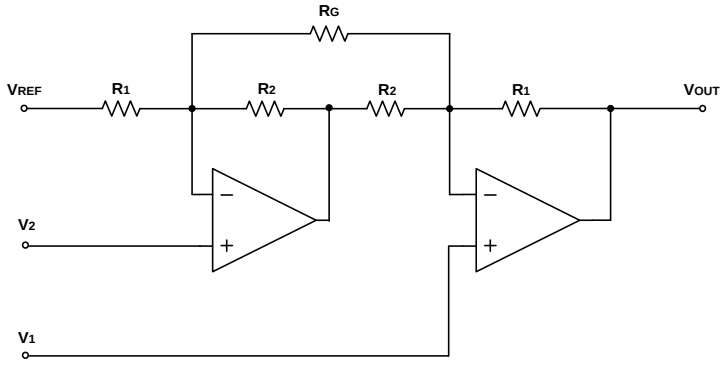
When R3 = R1, R2 = R4, $R_{SHUNT} << R1$

Figure 24 Dual Supply Operation Connections

Instrumentation Amplifier

The LMV321TP/358TP/324TP OPA is well suited for conditioning sensor signals in battery-powered applications. Figure 25 shows a two op-amp instrumentation amplifier, using the LMV321TP/358TP/324TP OPA.

The circuit works well for applications requiring rejection of Common Mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single voltage supply applications, V_{REF} is typically $V_{DD}/2$.



$$V_{OUT} = (V_1 - V_2)(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G}) + V_{REF}$$

Figure 25

Gain-of-100 Amplifier Circuit

Figure 26 shows a Gain-of-100 amplifier circuit using two LMV321TP/358TP/324TP OPAs. It draws 74 μA total current from supply rail, and has a −3 dB frequency at 100 kHz. Figure 27 shows the small signal frequency response of the circuit.

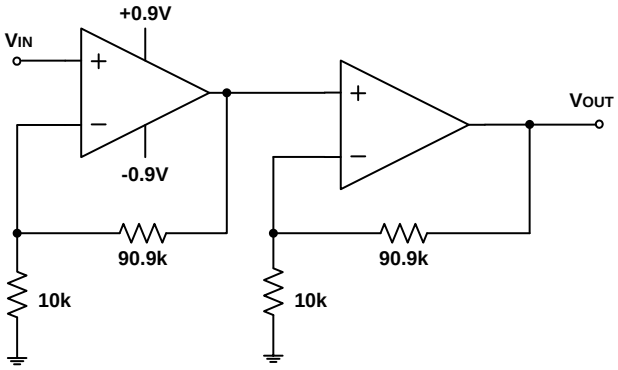


Figure 26 100 kHz, 74 μA Gain-of-100 Amplifier

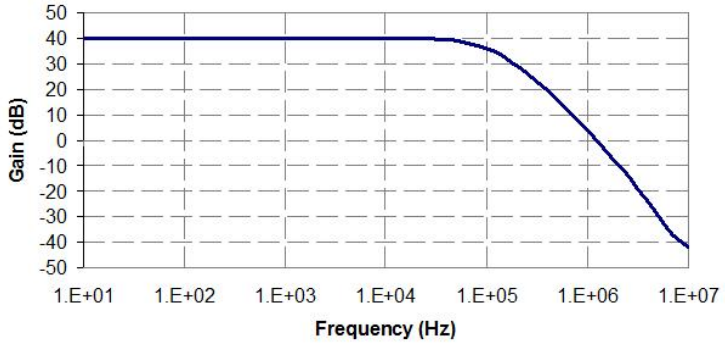


Figure 27 Frequency response of 100 kHz, 74 μA Gain-of-100 Amplifier

Buffered Chemical Sensor (pH) Probe

The LMV321TP/358TP/324TP OPA has input bias current in the pA range. This is ideal in buffering high impedance chemical sensors such as pH probe. As an example, the circuit in Figure 28 eliminates expansive low-leakage cables that that is required to connect pH probe to metering ICs such as ADC, AFE and/or MCU. A LMV321TP/358TP/324TP OPA and a lithium battery are housed in the probe assembly. A conventional low-cost coaxial cable can be used to carry OPA's output signal to subsequent ICs for pH reading.

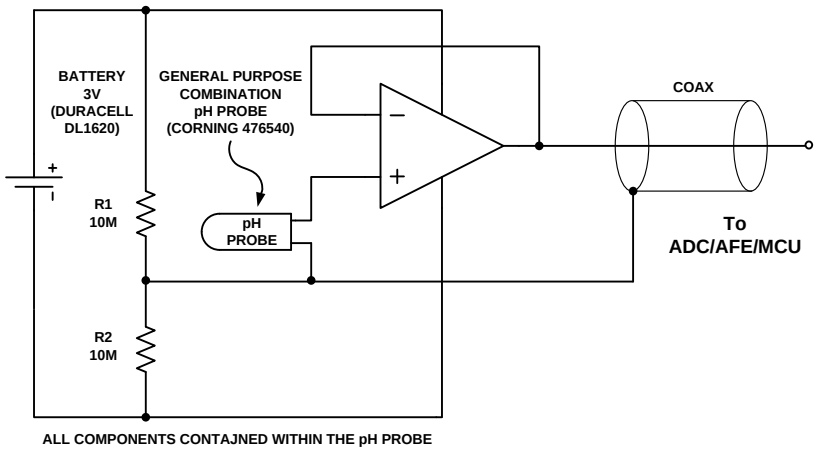


Figure 28 Buffer pH Probe

Two-Pole Micro-power Sallen-Key Low-Pass Filter

Figure 29 shows a micro-power two-pole Sallen-Key Low-Pass Filter with 400 Hz cut-off frequency. For best results, the filter's cut-off frequency should be 8 to 10 times lower than the OPA's crossover frequency. Additional OPA's phase margin shift can be avoided if the OPA's bandwidth-to-signal ratio is greater than 8. The design equations for the 2-pole Sallen-Key low-pass filter are given below with component values selected to set a 400 Hz low-pass filter cutoff frequency:

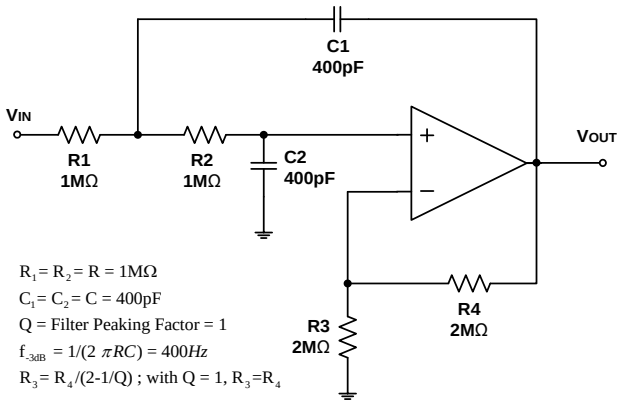


Figure 29

Portable Gas Sensor Amplifier

Gas sensors are used in many different industrial and medical applications. Gas sensors generate a current that is proportional to the percentage of a particular gas concentration sensed in an air sample. This output current flows through a load resistor and the resultant voltage drop is amplified. Depending on the sensed gas and sensitivity of the sensor, the output current can be in the range of tens of microamperes to a few milli-amperes. Gas sensor datasheets often specify a recommended load resistor value or a range of load resistors from which to choose.

There are two main applications for oxygen sensors – applications which sense oxygen when it is abundantly present (that is, in air or near an oxygen tank) and those which detect traces of oxygen in parts-per-million concentration. In medical applications, oxygen sensors are used when air quality or oxygen delivered to a patient needs to be monitored. In fresh air, the concentration of oxygen is 20.9% and air samples containing less than 18% oxygen are considered dangerous. In industrial applications, oxygen sensors are used to detect the absence of oxygen; for example, vacuum-packaging of food products.

The circuit in Figure 30 illustrates a typical implementation used to amplify the output of an oxygen detector. With the components shown in the figure, the circuit consumes less than 37 μA of supply current ensuring that small form-factor single- or button-cell batteries (exhibiting low mAh charge ratings) could last beyond the operating life of the oxygen sensor. The precision specifications of these amplifiers, such as their low offset voltage, low TC-VOS, low input bias current, high CMRR, and high PSRR are other factors which make these amplifiers excellent choices for this application.

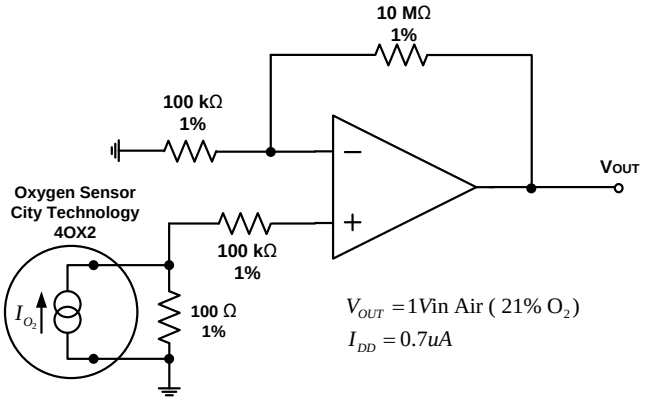
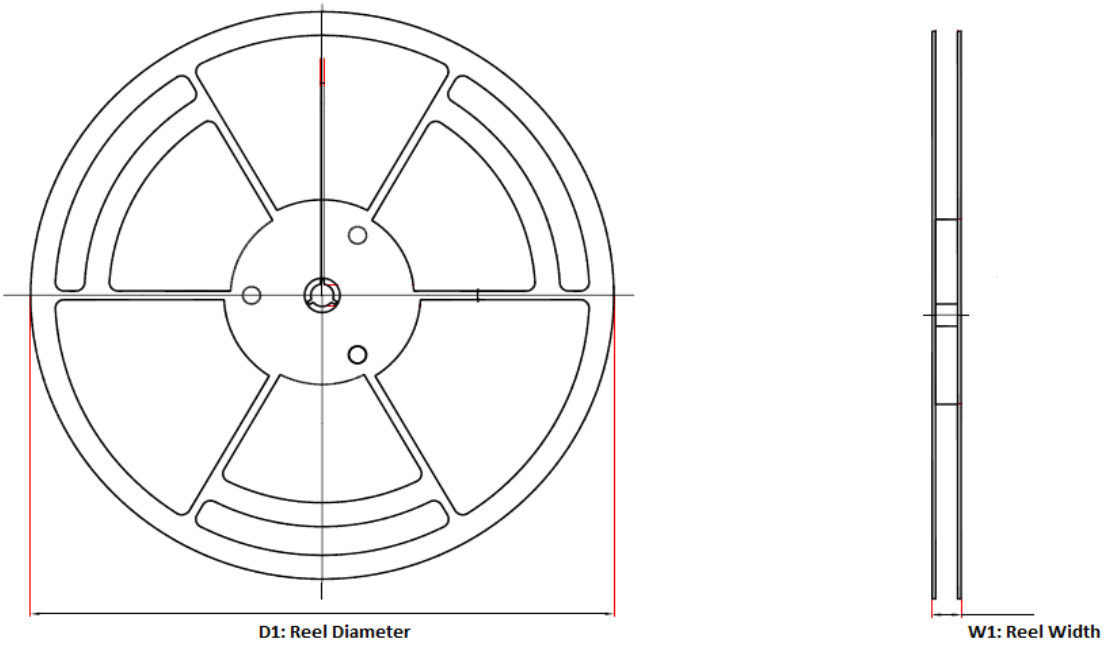

10 MΩ
1%
100 kΩ
1%
VOUT
Oxygen Sensor
City Technology
4OX2
100 kΩ
1%
100 Ω
1%
I_{O_2}
$V_{OUT} = 1V$in Air (21% O_2)
$I_{DD} = 0.7uA$

Figure 30

Tape and Reel Information

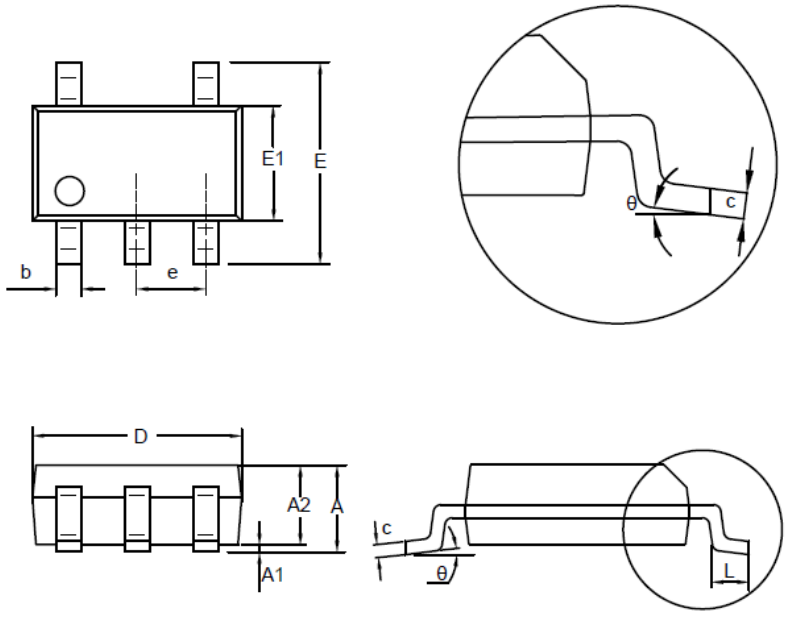


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
LMV321TP-CR	SOT353 (SC70-5)	178.0	12.3	2.4	2.5	1.2	4.0	8.0	Q3
LMV321TP-TR	SOT23-5	180.0	13.1	3.2	3.2	1.4	4.0	8.0	Q3
LMV358TP-SR	SOP8	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1
LMV358TP-FR	DFN2X2-8	180.0	13.1	2.3	2.3	1.1	4.0	8.0	Q1
LMV358TP-VR	MSOP8	330.0	17.6	5.2	3.3	1.5	8.0	12.0	Q1
LMV324TP-SR	SOP14	330.0	21.6	6.5	9.0	2.1	8.0	16.0	Q1
LMV324TP-TR	TSSOP14	330.0	17.6	6.8	5.4	1.2	8.0	12.0	Q1

Package Outline Dimensions

SOT23-5

Package Outline Dimensions S5T(SOT23-5-A)



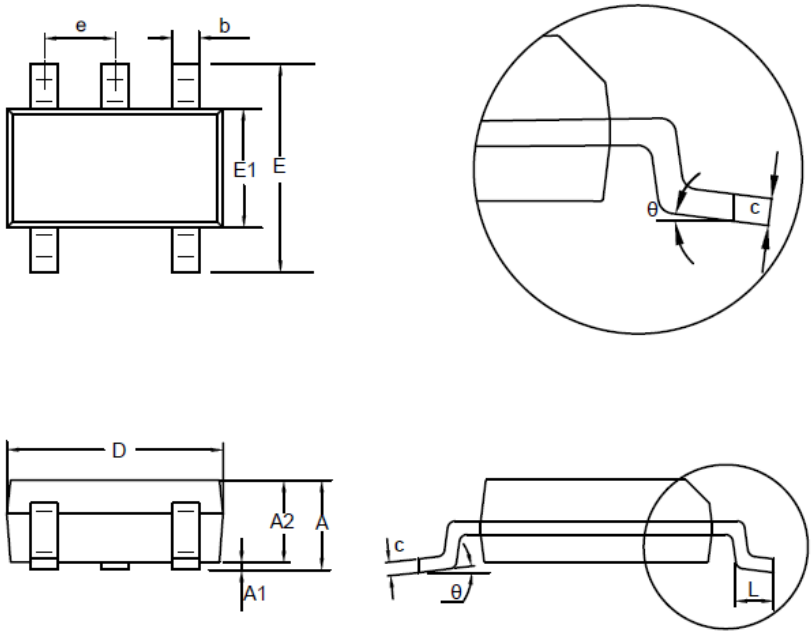
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

SOT353 (SC70-5)

Package Outline Dimensions SC5(SOT353-5-A)



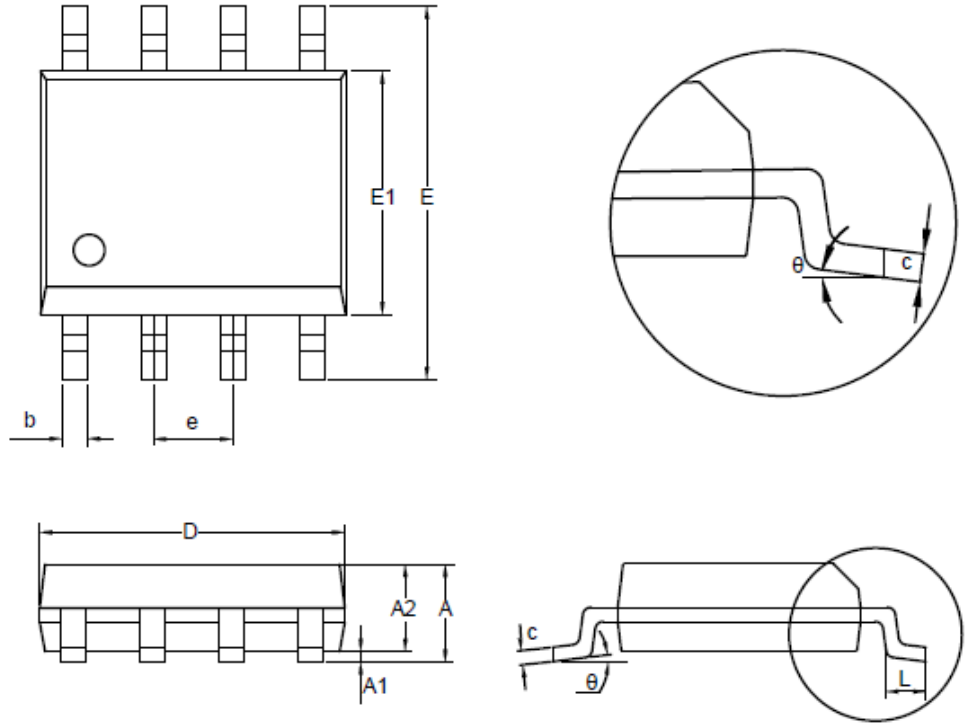
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.850	1.100	0.033	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	1.000	0.031	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.230	0.004	0.009
D	2.000	2.200	0.079	0.087
E	2.150	2.450	0.085	0.096
E1	1.150	1.350	0.045	0.053
e	0.650 BSC		0.026 BSC	
L	0.260	0.460	0.010	0.018
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

SOP8

Package Outline Dimensions SO1(SOP-8-A)



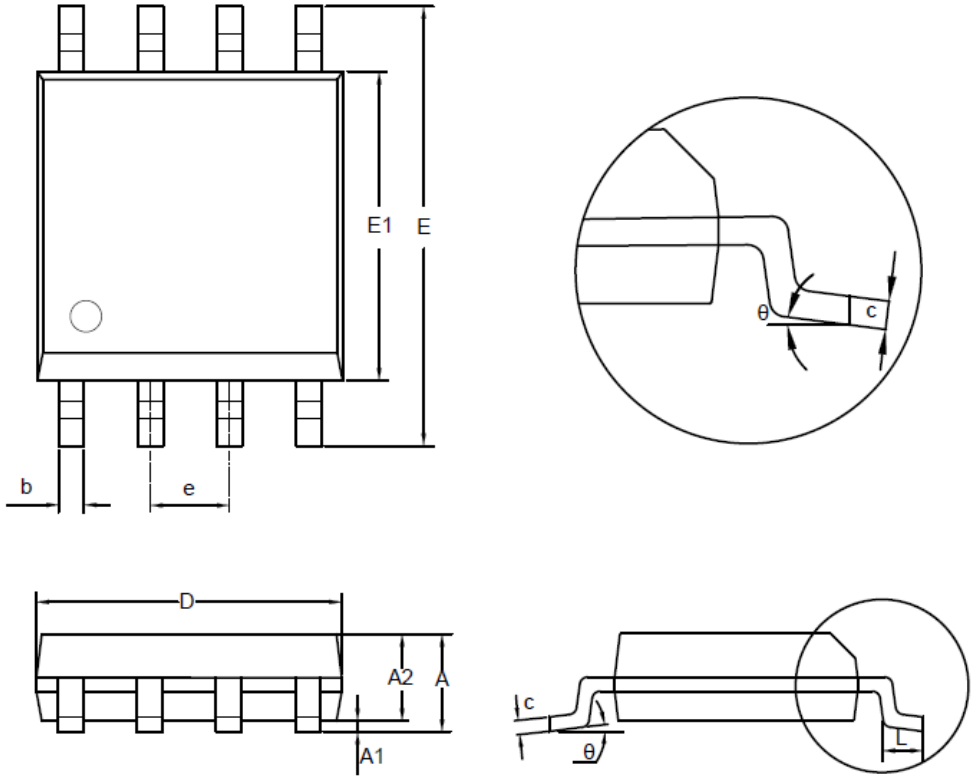
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

MSOP8

Package Outline Dimensions VS1(MSOP-8-A)

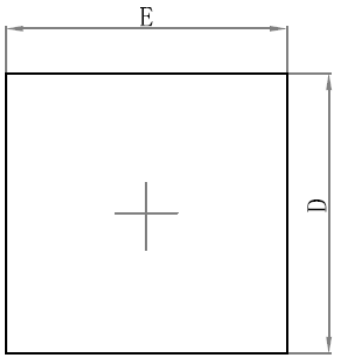


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

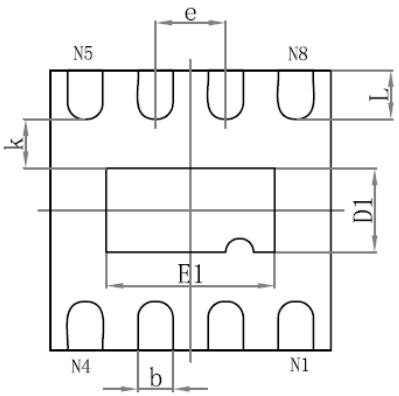
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

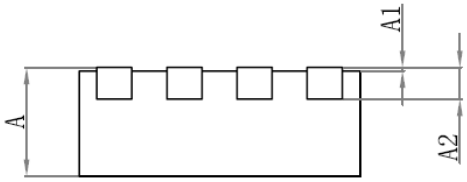
DFN2X2-8



Top View



Bottom View

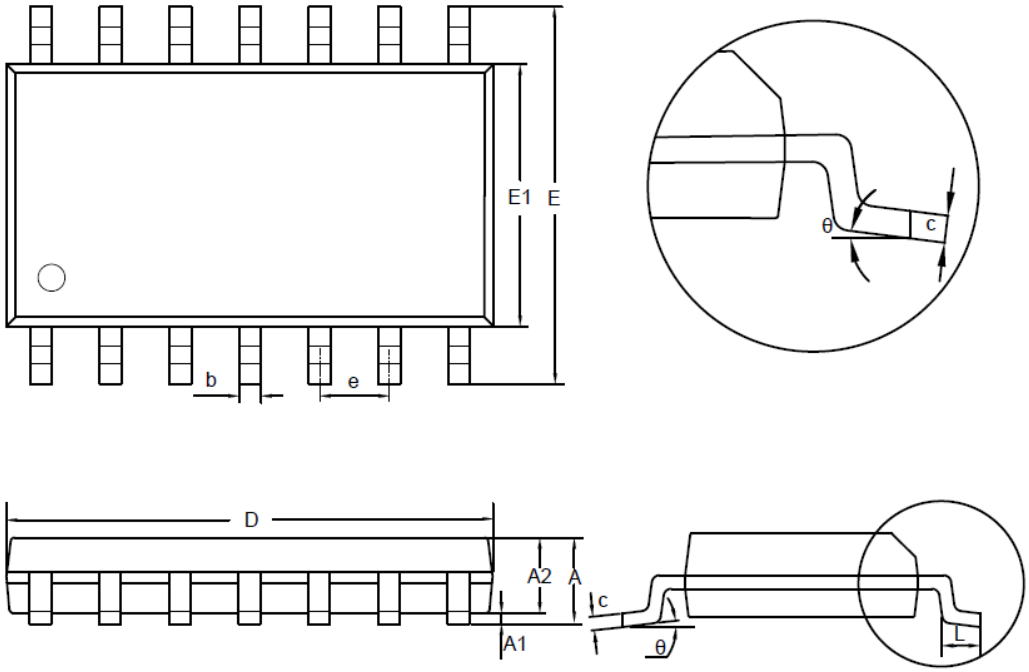


Side View

Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.9	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.153	0.203	0.253	0.006	0.008	0.010
b	0.18	0.24	0.30	0.007	0.009	0.012
D	1.9	2.0	2.1	0.075	0.079	0.083
E	1.9	2.0	2.1	0.075	0.079	0.083
D1	0.5	0.6	0.7	0.020	0.024	0.028
E1	1.1	1.2	1.3	0.043	0.047	0.051
e		0.50			0.20	
k	0.2			0.008		
L	0.25	0.35	0.45	0.010	0.014	0.018

SOP14

Package Outline Dimensions SO2(SOP-14-A)



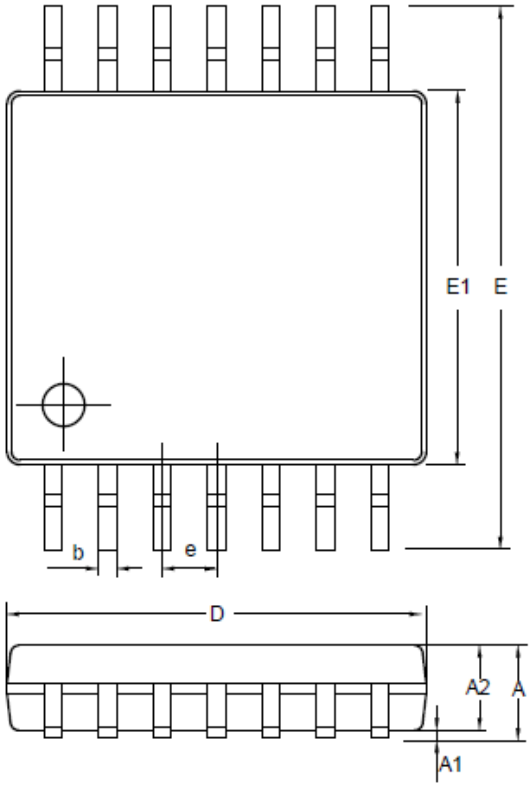
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0	8°	0	8°

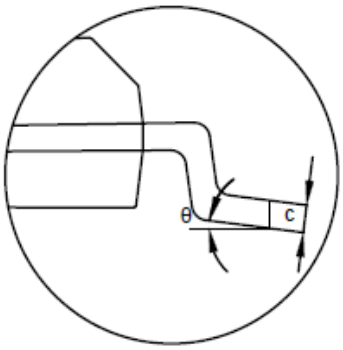
NOTES

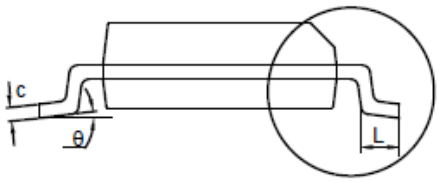
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

TSSOP14

Package Outline Dimensions TS2(TSSOP-14-A)







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
LMV321TP-CR	−40 to 125°C	SOT353 (SC70-5)	AC4YW (1)	MSL3	Tape and Reel, 3000	Green
LMV321TP-TR	−40 to 125°C	SOT23-5	AT4YW (1)	MSL1	Tape and Reel, 3000	Green
LMV358TP-SR	−40 to 125°C	SOP8	A42S	MSL3	Tape and Reel, 4000	Green
LMV358TP-VR	−40 to 125°C	MSOP8	A42V	MSL3	Tape and Reel, 3000	Green
LMV358TP-FR	−40 to 125°C	DFN2X2-8	A42	MSL3	Tape and Reel, 3000	Green
LMV324TP-SR	−40 to 125°C	SOP14	A44S	MSL3	Tape and Reel, 2500	Green
LMV324TP-TR	−40 to 125°C	TSSOP14	A44T	MSL3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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