

Features

- Meets the TIA/EIA- 422-B requirements
- High speed, up to 50Mbps data rate, and $t_{PLH} = t_{PHL} = 8$ ns typical
- Low pulse distortion, $t_{sk(p)} = 0.5$ ns Typical
- Wide power supply voltage 3.0V to 5.5V
- High output-drive current: ± 30 mA
- Low quiescent supply current: 30 μ A typical
- Differential output voltage in 5.0V VCC 3.9 V typical with 100- Ω Load
- Driver output short protection < 150mA
- Bus-Pin Protection:
 - ± 18 kV HBM protection
 - ± 9 kV IEC-Contact ESD
 - ± 15 kV IEC-Air ESD
- Pb-Free
- Package: SOP16, TSSOP16

Applications

- Field Transmitters: Temperature Sensors and Pressure Sensors
- Motor Controller/Position Encoder Systems
- Factory Automation
- Industrial/Process Control Networks

Description

3PEAK's TPT4031 is an enhanced RS422 device which meets standard TIA/EIA-422-B with strong ESD protection capability. The BUS-pin can pass ± 18 kV HBM-ESD, and ± 15 kV IEC-Air ESD protection. It works in wide power supply range: from 3.0V to 5.5V VCC, which provides quad driver for balanced communication. It also features the larger output voltage and higher data rate, the TPT4031 can generate 3.9V differential output with 100- Ω Load and 50Mbps data rate in 5.0V power supply, required by high speed field-bus applications. The device can generate 30mA high output drive current, with short protect function in some abnormal operations, the clamp current is less than 150mA.

The TPT4031's enable functions can control all four drivers and provide an active-high (G) or active-low (\bar{G}) enable input, and they provide the high-impedance state in the power-off condition, which only consume 6 μ A very low current.

The TPT4031 is available in an SOP16, and TSSOP16 package, and is characterized from -40°C to 125°C .

Functional block

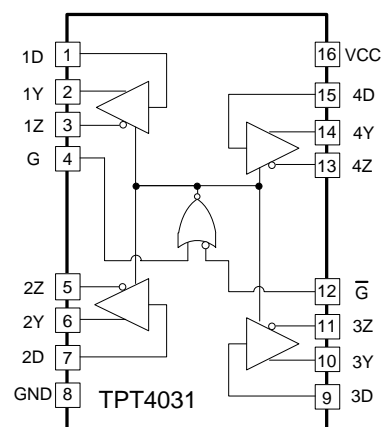


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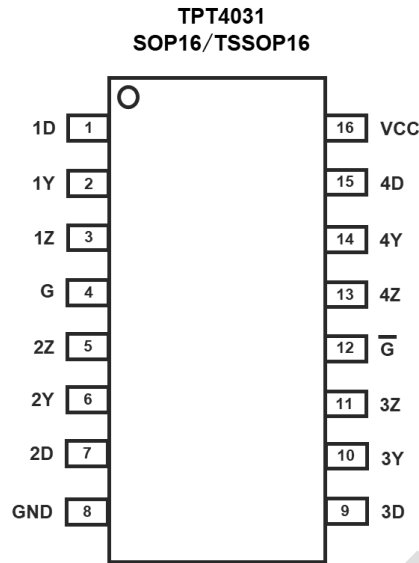
Revision History

Date	Revision	Notes
2020/11/18	Rev. Pre.0	Definition Version Pre.0
2021/1/7	Rev. Pre.1	Definition Version Pre.1, add electrical parameter
2021/1/12	Rev. Pre.2	Definition Version Pre.2, update Cpd data in 5V and 3.3V
2021/6/30	Rev. A	Release version

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TPT4031-SO3R	-40 to 125°C	16-Pin SOP	T4031	3	Tape and Reel, 2500
TPT4031-TS3R	-40 to 125°C	16-Pin TSSOP	T4031	3	Tape and Reel, 3000

Pin Configuration and Functions



Pin Functions

Table 1.

Pin		I/O	Description
1D	1	I	Driver 1 input
1Y	2	O	Driver 1 output
1Z	3	O	Driver 1 inverted output
G	4	I	Active high enable
2Z	5	O	Driver 2 inverted output
2Y	6	O	Driver 2 output
2D	7	I	Driver 2 input
GND	8	—	Ground pin
3D	9	I	Driver 3 input
3Y	10	O	Driver 3 output
3Z	11	O	Driver 3 inverted output
/G	12	I	Active low enable
4Z	13	O	Driver 3 inverted output
4Y	14	O	Driver 3 output
4D	15	I	Driver 3 input
VCC	16	—	Power pin

Absolute Maximum Ratings

Table 4.

Parameter	Description	Min	Max	Unit
VCC	Supply voltage ⁽²⁾	-0.5	7	V
V _I	Input voltage	-0.5	VCC + 0.5	V
V _{ID}	Differential input voltage	-7	12	V
V _O	Output voltage	-0.5	7	V
I _{IK} I _{OK}	Input or output clamp current		±20	mA
I _O	Output current		±150	mA
	VCC current		200	mA
	GND current	-200		mA
T _J	Operating virtual junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

* **Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(1) This data was taken with the JEDEC low effective thermal conductivity test board.

(2) This data was taken with the JEDEC standard multilayer test boards.

Recommended Operating Conditions

Table 5.

Parameter	Description	Min	Max	Unit
VCC	Supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)	2	VCC	V
V _{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)	0	0.8	V
V _{ID}	Differential input voltage	-7	7	V
R _L	Differential load resistance	100		Ω
T _A	Operating ambient temperature	-40	125	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

ESD, Electrostatic Discharge Protection

Table 2.

		Value	Unit
IEC-61000-4-2, Contact Discharge	Bus Pin	±9	kV
IEC-61000-4-2, Air-Gap Discharge	Bus Pin	±15	kV
HBM, per ANSI/ESDA/JEDEC JS-001 / ANSI/ESD STM5.5.1	Bus Pin	±18	kV
	All Pin Except Bus Pin	±7	kV
CDM, per ANSI/ESDA/JEDEC JS-002	All Pin	±1.5	kV

Thermal Information

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
16-Pin TSSOP	115	48	°C/W
16-Pin SOP	91	31	°C/W

Note:

- (1) Parameter is provided from 1S0P PCB per JEDEC standard
- (2) θ_{JA} , θ_{JC} data is only for reference by design simulation

Electrical Characteristics

Typical value is in VCC = 5.0V, TA = +25°C, RL = 100Ω to GND, unless otherwise noted.

Table 4.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input Electrical Specifications						
V _{IK}	Enable-input clamp voltage	I _o = 18 mA			-1.5	V
V _{IH}	Logic Input High Voltage	Dx, G, /G	2.0			V
V _{IL}	Logic Input Low Voltage	Dx, G, /G			0.8	V
V _{OH}	High-level output voltage	I _o = -20 mA	2.4	4.6		V
V _{OL}	Low-level output voltage	I _o = 20 mA		0.21	0.4	V
V _{OD}	Differential output voltage magnitude	R _L = 100 Ω, see Figure 1	2.4	3.9		V
		No load, see Figure 1	4.0	5.0		V
Δ V _{OD}	Change in magnitude of V _{OD} ⁽¹⁾	R _L = 100 Ω, see Figure 1		0	±0.4	V
		No load, see Figure 1		0	±0.4	V
V _{OC}	Common-mode output voltage	R _L = 100 Ω, see Figure 1		2.35	3.0	V
Δ V _{OC}	Change in magnitude of V _{OC} ⁽¹⁾	R _L = 100 Ω, see Figure 1		0	±0.4	V
I _I	Input current	V _I = VCC or GND			±10	uA
I _{O(off)}	Driver output current with power off	VCC=0, V _O = 6 V		6	50	uA
		VCC=0, V _O = -0.25 V		-6	-50	uA
I _{OS}	Driver output short-circuit current	Bus pin Y, Z short current	-30		-150	mA
		Bus pin Y or Z short to V _O = VCC or GND ⁽²⁾	-30		-150	mA
I _{OZ}	High-impedance off-state output current	V _O = 6 V			20	uA
		V _O = -0.25 V			-100	uA
I _{CC}	Quiescent supply current	I _o =0, V _I = 0 or 5 V		30	50	uA
C _i	Input capacitance ⁽²⁾			12		pF

***Note:**

(1). Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

(2). Provided by bench test and design simulation

AC Electrical Specifications

Typical value is in VCC = 5.0V, TA = +25°C, RL = 100Ω to GND

Table 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{PLH}	Propagation delay time, low-to-high-level output	SW is open, see Figure 2 ⁽¹⁾	3	8	12	ns
t _{PHL}	Propagation delay time, high-to-low-		3	8	12	ns

	level output					
tsk(p)	Pulse skew time ($ t_{PLH} - t_{PHL} $)	SW is open, see Figure 2		0.5	5	ns
tr	Differential output rise times	SW is open, see Figure 2		6.5	10	ns
tr	Differential output fall times			6.5	10	ns
tPZH	Output enable time to high level	SW is closed, see Figure 3		12	20	ns
tPZL	Output enable time to low level			14	20	ns
tPHZ	Output disable time from high level	SW is closed, see Figure 3		9	20	ns
tPLZ	Output disable time from low level			10	17	ns
Cpd	Power dissipation capacitance	VCC=5V, SW is open, see Figure 2 ⁽²⁾		260		pF

***Note:**

- (1). Provided by bench test and design simulation
- (2). Reference IS = ICC + Cpd*VCC*f (f is input data rate), provided @1MHz (typical) by bench test

Electrical Characteristics (Continue)

Typical value is in VCC = 3.3V, TA = +25°C, RL = 100Ω to GND, unless otherwise noted.

Table 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input Electrical Specifications						
V _{IK}	Enable-input clamp voltage	I _o = 18 mA			-1.5	V
V _{IH}	Logic Input High Voltage	Dx, G, /G	2.0			V
V _{IL}	Logic Input Low Voltage	Dx, G, /G			0.8	V
V _{OH}	High-level output voltage	I _o = -20 mA	2.0	2.9		V
V _{OL}	Low-level output voltage	I _o = 20 mA		0.22	0.4	V
V _{OD}	Differential output voltage magnitude	R _L = 100 Ω, see Figure 1	1.9	2.5		V
		No load, see Figure 1	2.5	3.27		V
Δ V _{OD}	Change in magnitude of V _{OD} ⁽¹⁾	R _L = 100 Ω, see Figure 1		0	±0.4	V
		No load, see Figure 1		0	±0.4	V
V _{OC}	Common-mode output voltage	R _L = 100 Ω, see Figure 1		1.54	2.0	V
Δ V _{OC}	Change in magnitude of V _{OC} ⁽¹⁾	R _L = 100 Ω, see Figure 1		0	±0.4	V
I _I	Input current	V _I = VCC or GND			±10	uA
I _O (off)	Driver output current with power off	VCC=0, V _O = 6 V		6	50	uA
		VCC=0, V _O = -0.25 V		-6	-50	uA
I _{OS}	Driver output short-circuit current	Bus pin Y, Z short current	-30		-150	mA
		Bus pin Y or Z short to V _O = VCC or GND ⁽²⁾	-30		-150	mA
I _{OZ}	High-impedance off-state output current	V _O = 6 V			20	uA
		V _O = -0.25 V			-100	

I _{cc}	Quiescent supply current	I _o =0, V _i = 0 or 3.3 V		20	40	uA
C _i	Input capacitance ⁽⁵⁾			12		pF

***Note:**

- (1). $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
- (2). Provided by bench test and design simulation

AC Electrical Specifications

Typical value is in VCC = 3.3V, TA = +25°C, RL = 100Ω to GND, unless otherwise noted.

Table 11.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{PLH}	Propagation delay time, low-to-high-level output	SW is open, see Figure 2	3	8	12	ns
t _{PHL}	Propagation delay time, high-to-low-level output		3	8	12	ns
tsk(p)	Pulse skew time (t _{PLH} - t _{PHL})	SW is open, see Figure 2 ⁽¹⁾		0.5	5	ns
t _r	Differential output rise times	SW is open, see Figure 2 ⁽¹⁾		6.5	10	ns
t _f	Differential output fall times			6.5	10	ns
t _{PZH}	Output enable time to high level	SW is closed, see Figure 3		13.5	23	ns
t _{PZL}	Output enable time to low level			16.5	23	ns
t _{PHZ}	Output disable time from high level	SW is closed, see Figure 3		11	23	ns
t _{PLZ}	Output disable time from low level			14	23	ns
C _{pd}	Power dissipation capacitance	SW is open, see Figure 2 ⁽²⁾		112		pF

***Note:**

- (1). Parameter is provided by lab bench test and design simulation
- (2). Reference IS = ICC + Cpd*VCC*f (f is input data rate), provided @1MHz (typical) by bench test

Test Circuits and Waveforms

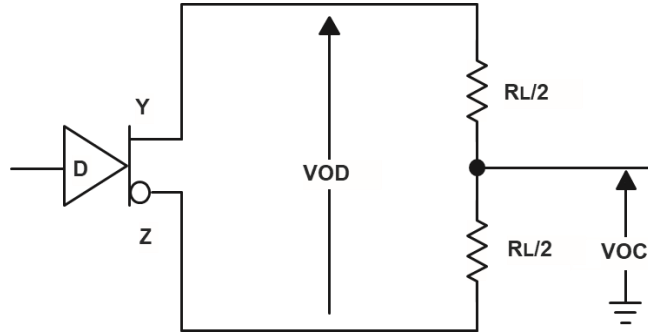


Figure 1 VOD & VOC with Common Mode Load

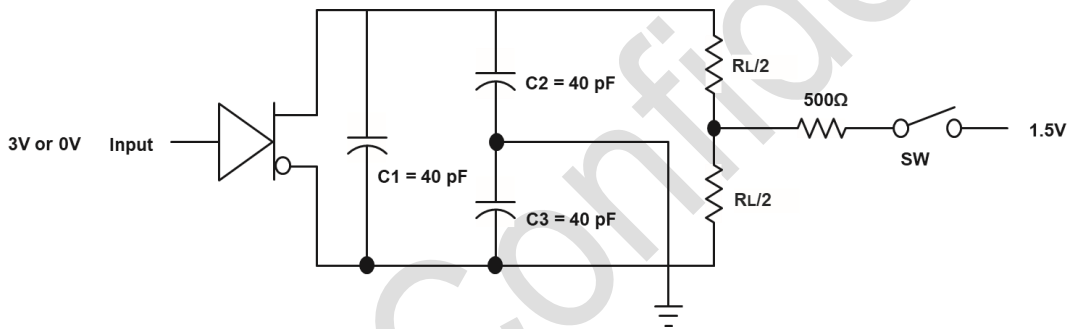


Figure 2A. Driver Propagation Delay and Differential Transition Times -- Test Circuit

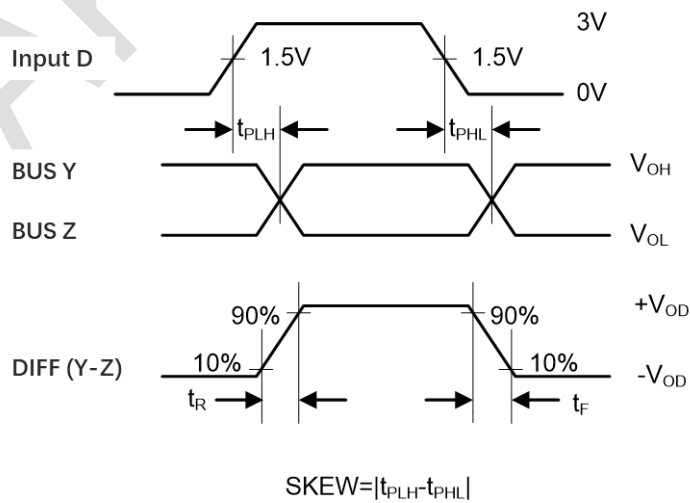


Figure 2B. Driver Propagation Delay and Differential Transition Times Measurement Points

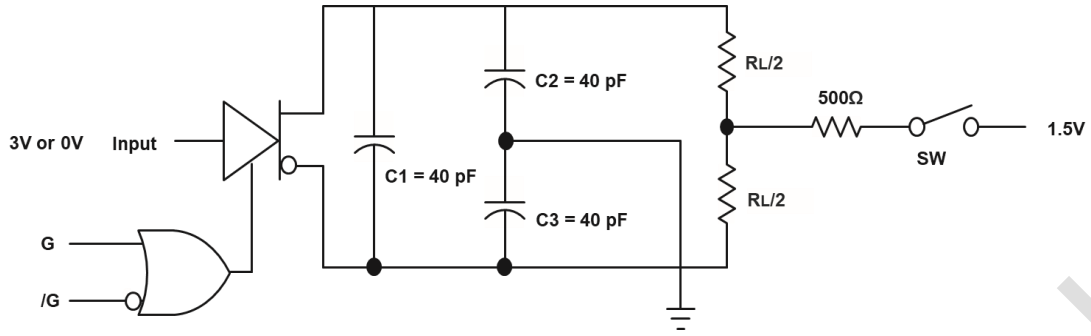


Figure 3A. Driver Enable and Disable Times -- Test Circuit

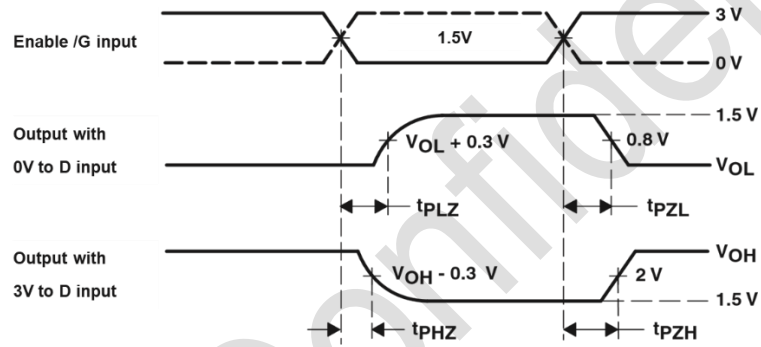


Figure 3B. Driver Enable and Disable Times -- Measurement Points

Theory of Operation

Overview

3PEAK's TPT4031 is a quad differential driver, which is designed to meet the requirements of TIA/EIA-422-B, and it usually communicates over the long wires in field bus applications. The TPT4031 has the strong ESD protection capability, the BUS-pin can pass $\pm 18\text{kV}$ HBM-ESD, and $\pm 9\text{ kV}$ IEC-Contact ESD protection. It works in wide power supply range: from 3.0V to 5.5V VCC, which provides quad driver for balanced communication. It also features the larger output voltage and higher data rate, the TPT4031 can generate 3.9V differential output with 100- Ω Load and 50Mbps data rate in 5.0V power supply, required by high speed field-bus applications. The device can generate 30mA high output drive current, with short protect function in some abnormal operations, the clamp current is less than 150mA. In the high-impedance state with power-off condition, TPT4031 only consumes 6 μA very low current.

Function block diagram

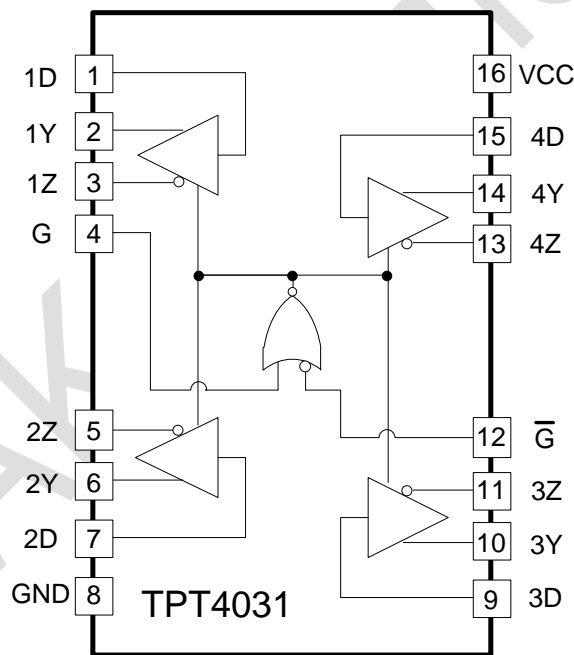


Figure 4. Function block diagram

Feature Description

Active-High in G and Active-Low in /G

The G and /G logic inputs can configure the device to select transmitter output status, and set a logic high on the G pin or a logic low on the /G pin to enable the device in normal operation mode, and it is easy to configure the logic from a controller or microprocessor.

Power supply

Both the logic and transmitters operate from a single power supply in wide range: 3.0 ~ 5.5V, making designs much more easily. The line quad drivers can operate off the same rail as the host controller or a similar low voltage supply, thus simplifying power structure. The 5.0V power supply is recommended to get better performance, especially in high data rate up-to 50Mbps.

Device Functional Modes

Table 12.

Input D	Enables		Outputs	
	G	/G	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

Note:

H = High level,

L = Low level,

X = Irrelevant,

Z = High impedance (off)

Application and Implementation

Application Information

A typical system usually contain the drivers, receivers, and transceivers complied with RS-422, to reduce reflections in the transmission line, requires the proper cable termination for highly reliable applications. Only one driver on the bus is allowed per RS422 standard, as termination is used in circuit and it is usually placed at the end of the cable near the last receiver. In order to get the good performance and low cost of the application, and decide the type of termination. The different types of termination are unterminated lines, parallel termination, AC termination, and multipoint termination. For laboratory experiments, around 50 meter of 100-Ω, twisted-pair cable, a single driver and receiver, 3PEAK TPT4031 and TPT4032 were tested at room temperature with in 5.0V supply voltage.

Typical Application

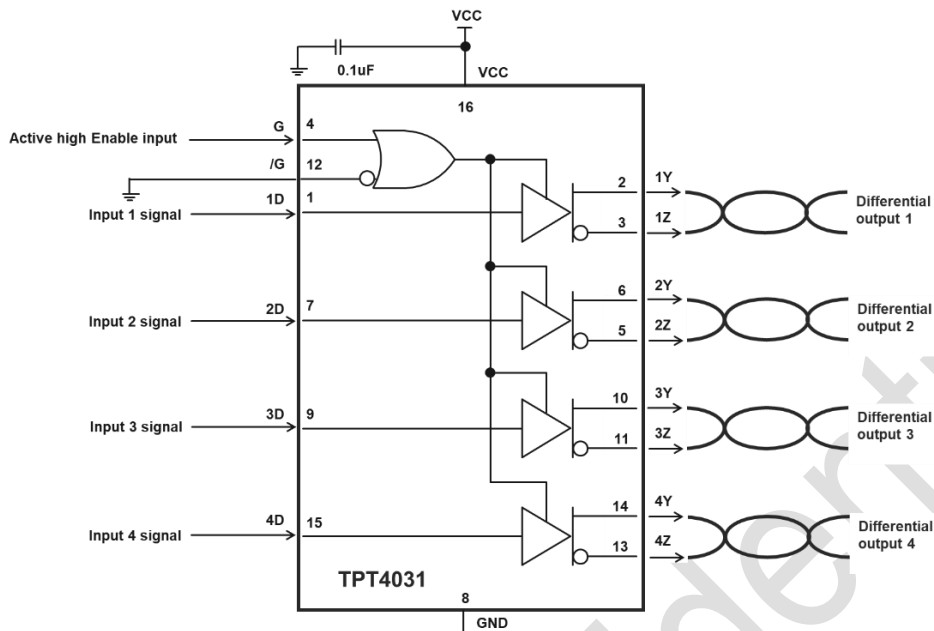


Figure 5. Typical application reference circuit

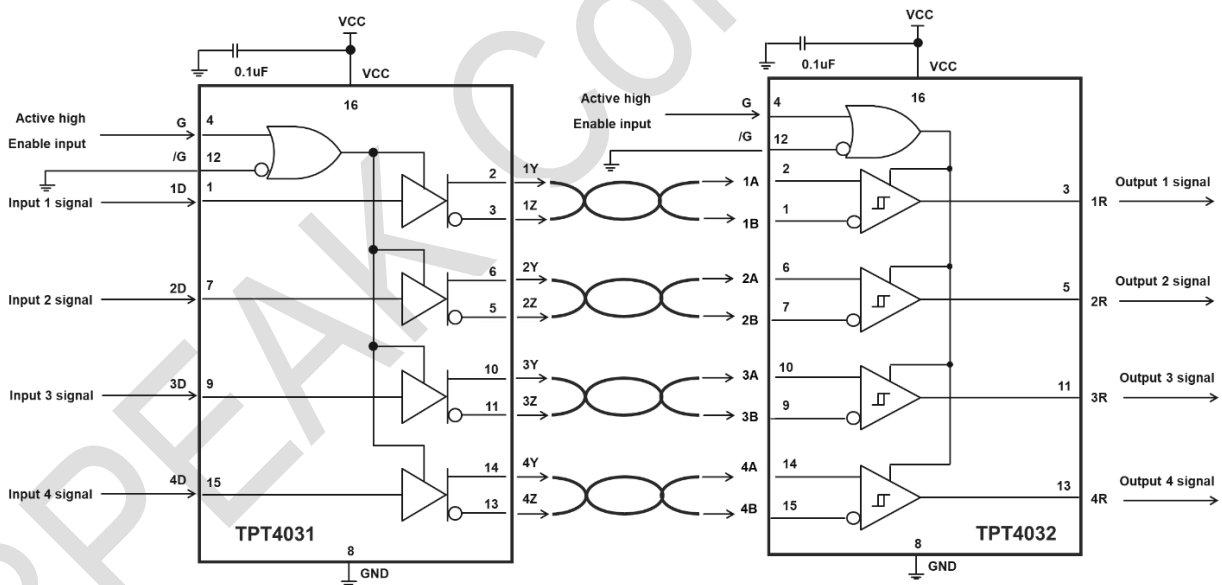
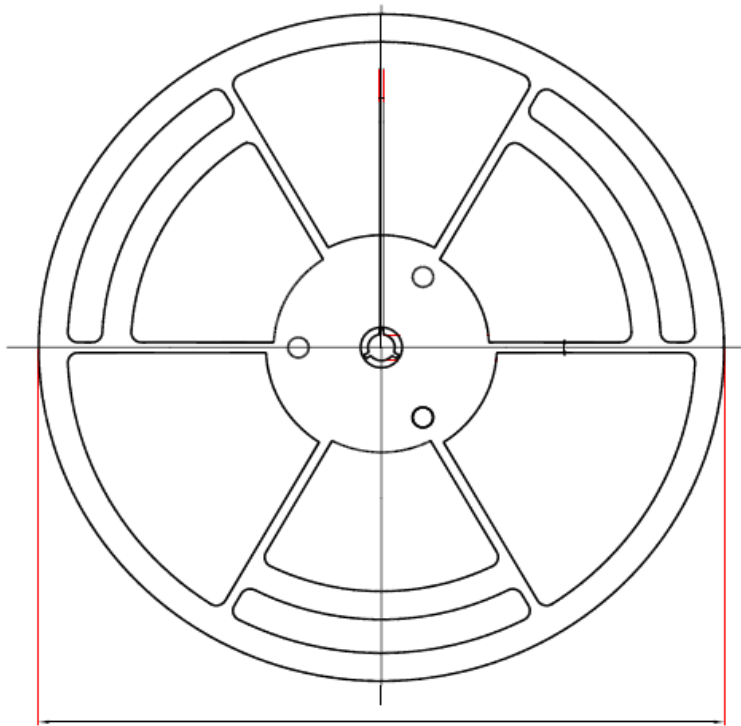


Figure 6. Typical application reference circuit

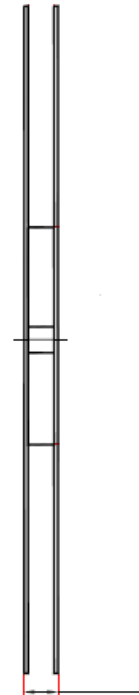
Resistor and capacitor termination values are shown for each lab experiment, but vary from different system. For example, the termination resistor, R_T , must be within 20% of the characteristic impedance, Z_o , of the cable and can vary from about 80 Ω to 120 Ω .

Place 0.1 μ F bypass capacitors is required close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies.

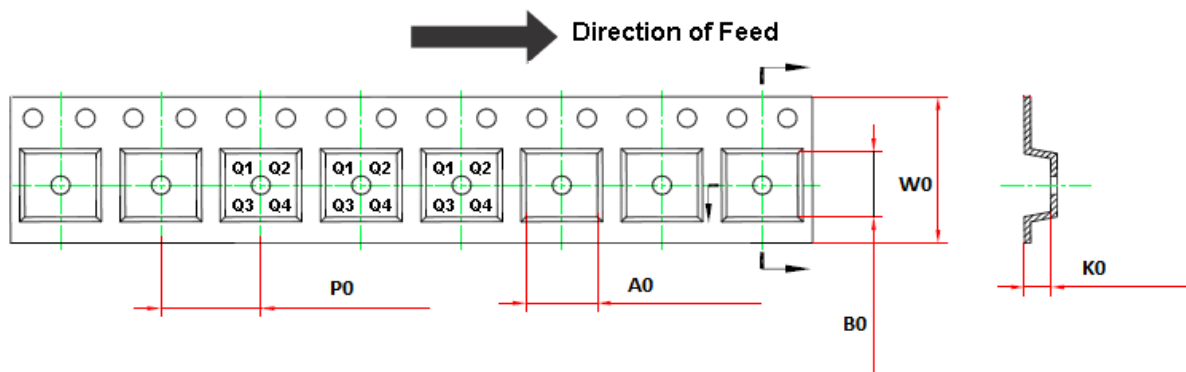
Tape and Reel Information



D1: Reel Diameter



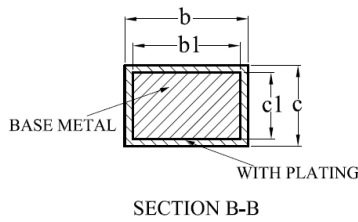
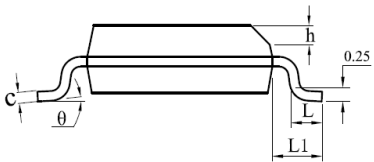
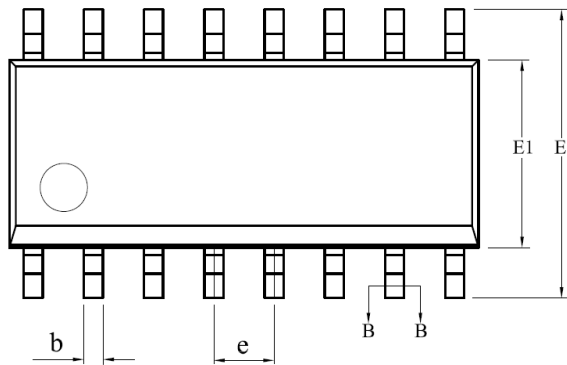
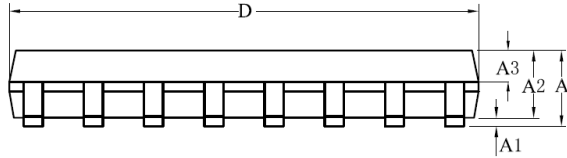
W1: Reel Width



Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
TPT4031-SO3R	SOP16	330	21.6	6.7	10.4	2.1	8.0	16.0	Q1
TPT4031-TS3R	TSSOP16	330	17.6	6.8	5.4	1.3	8.0	12.0	Q1

Package Outline Dimensions

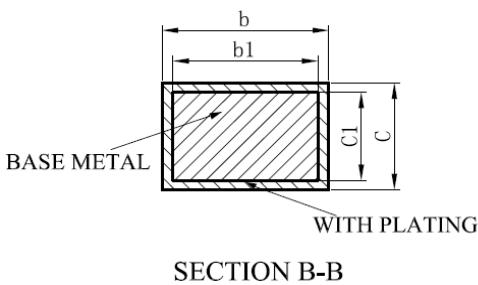
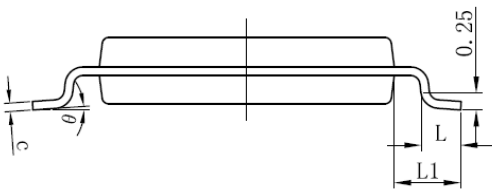
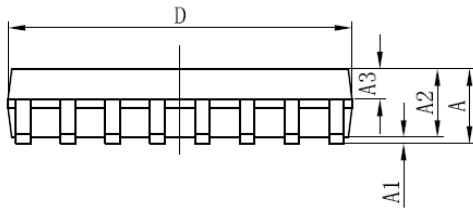
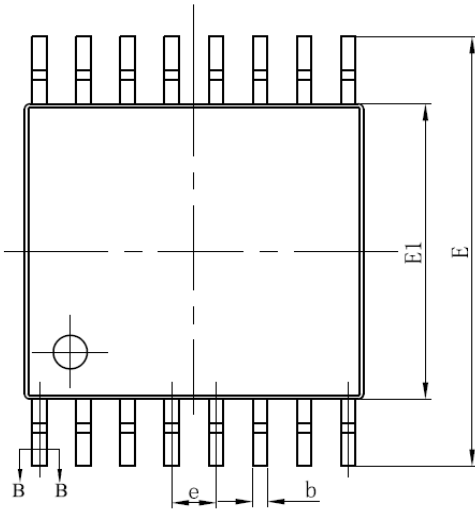
SO3R (SOP16)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Package Outline Dimensions

TS3R (TSSOP16)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°