MC74HC74A

Dual D Flip-Flop with Set and Reset

### High−Performance Silicon−Gate CMOS

The MC74HC74A is identical in pinout to the LS74. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two D flip−flops with individual Set, Reset, and Clock inputs. Information at a D−input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and $\overline{Q}$ outputs are available from each flip−flop. The Set and Reset inputs are asynchronous.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 128 FETs or 32 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant
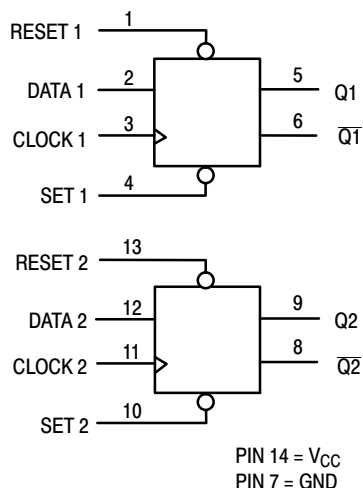
ON Semiconductor®

SOIC−14 NB
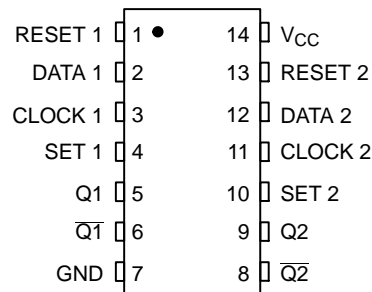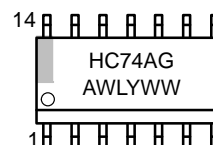**D SUFFIX**
CASE 751A

TSSOP−14
DT SUFFIX
CASE 948G

PIN ASSIGNMENT

RESET 1	1 ●		14	V_{CC}
DATA 1	2		13	RESET 2
CLOCK 1	3		12	DATA 2
SET 1	4		11	CLOCK 2
Q1	5		10	SET 2
$\overline{Q1}$	6		9	Q2
GND	7		8	$\overline{Q2}$

MARKING DIAGRAMS

14
HC74AG
AWLYWW
1

SOIC−14 NB

14
HC
74A
ALYW▪
1
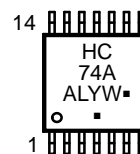
TSSOP−14

A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

LOGIC DIAGRAM

RESET 1 — 1
DATA 1 — 2
CLOCK 1 — 3
SET 1 — 4
Q1 — 5
$\overline{Q1}$ — 6

RESET 2 — 13
DATA 2 — 12
CLOCK 2 — 11
SET 2 — 10
Q2 — 9
$\overline{Q2}$ — 8

PIN 14 = V_{CC}
PIN 7 = GND

August, 2014 – Rev. 14

1

MC74HC74A

FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	⌐	X	No Change	

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or TSSOP Package)	 260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
†Derating: SOIC Package: −7 mW/°C from 65° to 125°C
               TSSOP Package: −6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figures 1, 2, 3)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

MC74HC74A

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V$_{CC}$ V	Guaranteed Limit			Unit
				−55 to 25°C	≤ 85°C	≤ 125°C	
V$_{IH}$	Minimum High–Level Input Voltage	V$_{out}$ = 0.1 V or V$_{CC}$ − 0.1 V |I$_{out}$| ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V$_{IL}$	Maximum Low–Level Input Voltage	V$_{out}$ = 0.1 V or V$_{CC}$ − 0.1 V |I$_{out}$| ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V$_{OH}$	Minimum High–Level Output Voltage	V$_{in}$ = V$_{IH}$ or V$_{IL}$ |I$_{out}$| ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V$_{in}$ = V$_{IH}$ or V$_{IL}$ |I$_{out}$| ≤ 2.4 mA |I$_{out}$| ≤ 4.0 mA |I$_{out}$| ≤ 5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V$_{OL}$	Maximum Low–Level Output Voltage	V$_{in}$ = V$_{IH}$ or V$_{IL}$ |I$_{out}$| ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V$_{in}$ = V$_{IH}$ or V$_{IL}$ |I$_{out}$| ≤ 2.4 mA |I$_{out}$| ≤ 4.0 mA |I$_{out}$| ≤ 5.2 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I$_{in}$	Maximum Input Leakage Current	V$_{in}$ = V$_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I$_{CC}$	Maximum Quiescent Supply Current (per Package)	V$_{in}$ = V$_{CC}$ or GND I$_{out}$ = 0 μA	6.0	2.0	20	80	μA

AC ELECTRICAL CHARACTERISTICS (C$_L$ = 50 pF, Input t$_r$ = t$_f$ = 6.0 ns)

Symbol	Parameter	V$_{CC}$ V	Guaranteed Limit			Unit
			− 55 to 25°C	≤ 85°C	≤ 125°C	
f$_{max}$	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t$_{PLH}$, t$_{PHL}$	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	2.0 3.0 4.5 6.0	100 75 20 17	125 90 25 21	150 120 30 26	ns
t$_{PLH}$, t$_{PHL}$	Maximum Propagation Delay, Set or Reset to Q or $\overline{Q}$ (Figures 2 and 4)	2.0 3.0 4.5 6.0	105 80 21 18	130 95 26 22	160 130 32 27	ns
t$_{TLH}$, t$_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
C$_{in}$	Maximum Input Capacitance	—	10	10	10	pF

		Typical @ 25°C, V$_{CC}$ = 5.0 V	
C$_{PD}$	Power Dissipation Capacitance (Per Flip–Flop)*	32	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0 3.0 4.5 6.0	80 35 16 14	100 45 20 17	120 55 24 20	ns
t_h	Minimum Hold Time, Clock to Data (Figure 3)	2.0 3.0 4.5 6.0	3.0 3.0 3.0 3.0	3.0 3.0 3.0 3.0	3.0 3.0 3.0 3.0	ns
t_{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0 3.0 4.5 6.0	8.0 8.0 8.0 8.0	8.0 8.0 8.0 8.0	8.0 8.0 8.0 8.0	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 3.0 4.5 6.0	60 25 12 10	75 30 15 13	90 40 18 15	ns
t_w	Minimum Pulse Width, Set or Reset (Figure 2)	2.0 3.0 4.5 6.0	60 25 12 10	75 30 15 13	90 40 18 15	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figures 1, 2, 3)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

ORDERING INFORMATION

Device	Package	Shipping[†]
MC74HC74ADG	SOIC−14 NB (Pb−Free)	55 Units / Rail
NLV74HC74ADG*	SOIC−14 NB (Pb−Free)	55 Units / Rail
MC74HC74ADR2G	SOIC−14 NB (Pb−Free)	2500 / Tape & Reel
NLV74HC74ADR2G*	SOIC−14 NB (Pb−Free)	2500 / Tape & Reel
MC74HC74ADTR2G	TSSOP−14 (Pb−Free)	2500 / Tape & Reel
NLV74HC74ADTR2G*	TSSOP−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MC74HC74A

SWITCHING WAVEFORMS
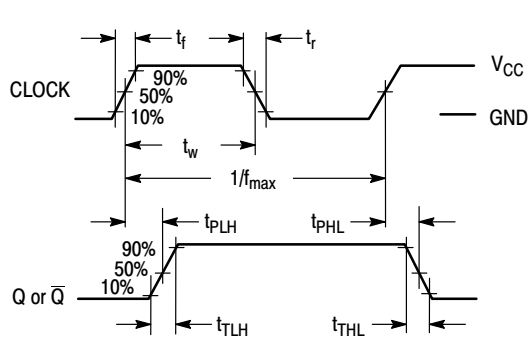
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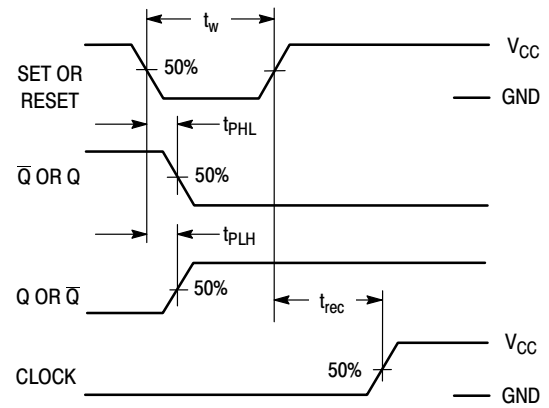
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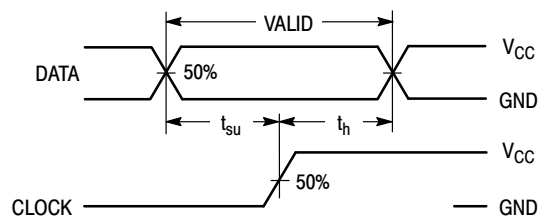
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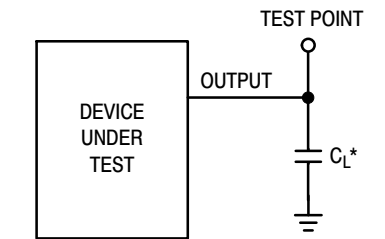
*Includes all probe and jig capacitance

Figure 4.
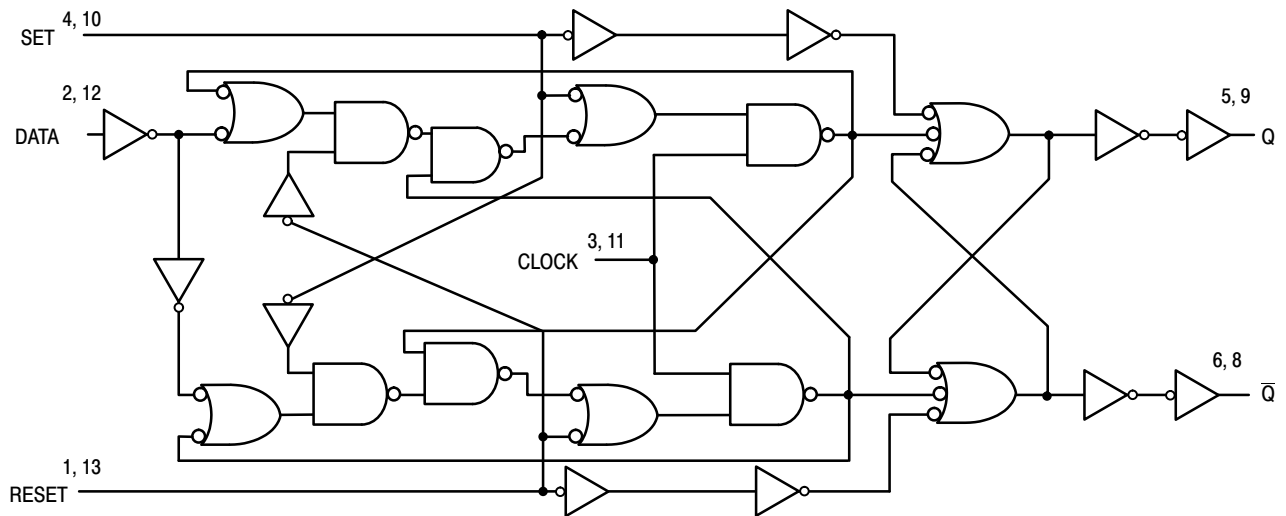
Figure 5. EXPANDED LOGIC DIAGRAM
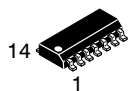
SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

14
1

SCALE 1:1
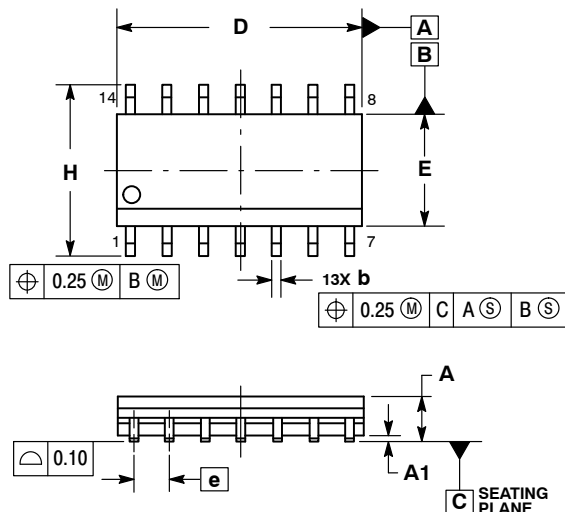
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DETAIL A

DETAIL A

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

13X b

0.25 (M) C A (S) B (S)

0.25 (M) B (M)

0.10

SEATING PLANE

X 45 °

SOLDERING FOOTPRINT*

6.50

14X 1.18

1.27 PITCH

14X 0.58

DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

14

XXXXXXXXXG
AWLYWW

1

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.
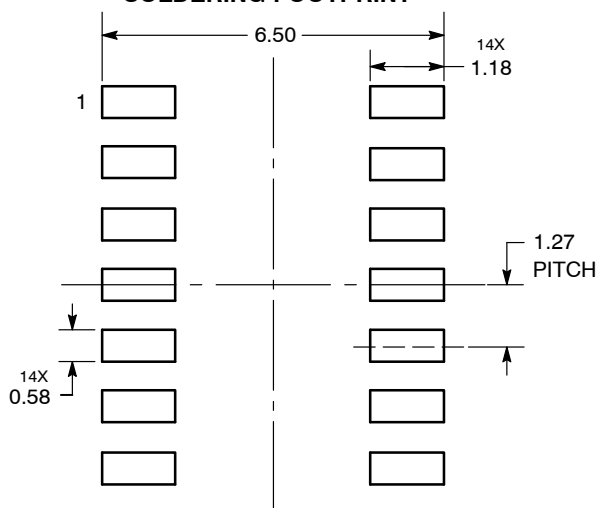
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

| DOCUMENT NUMBER:	98ASB42565B		
DESCRIPTION:	SOIC−14 NB		PAGE 1 OF 2

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−14 NB		PAGE 2 OF 2

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

14

SCALE 2:1

1

14X **K** REF

⊕ | 0.10 (0.004) Ⓜ | T | U Ⓢ | V Ⓢ

⌓ | 0.15 (0.006) | T | U Ⓢ

2X **L/2**

L

**PIN 1
IDENT.**

14   8

1   7

B
−U−

A
−V−

⌓ | 0.15 (0.006) | T | U Ⓢ

DETAIL E

N

0.25 (0.010)

M

N

F

SECTION N−N

K

K1

J J1

C

⌓ | 0.10 (0.004)

−T− **SEATING
PLANE**

D   **G**   **H**

DETAIL E

−W−
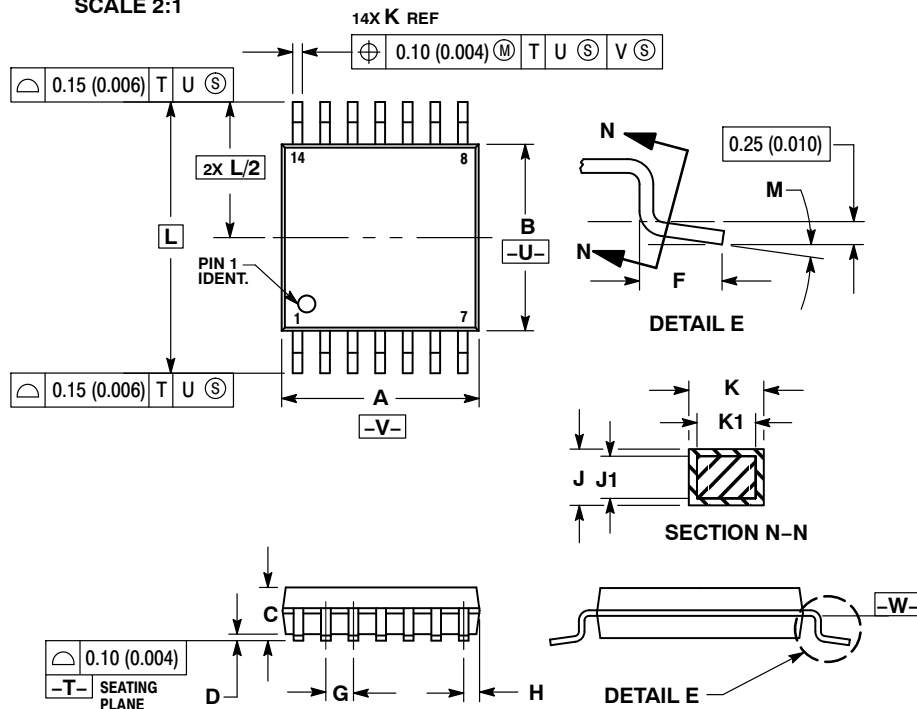
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

**GENERIC
MARKING DIAGRAM***

14

XXXX
XXXX
ALYW▪

1
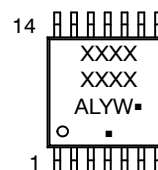
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

SOLDERING FOOTPRINT

7.06

1

0.65
PITCH

14X
0.36

14X
1.26

DIMENSIONS: MILLIMETERS
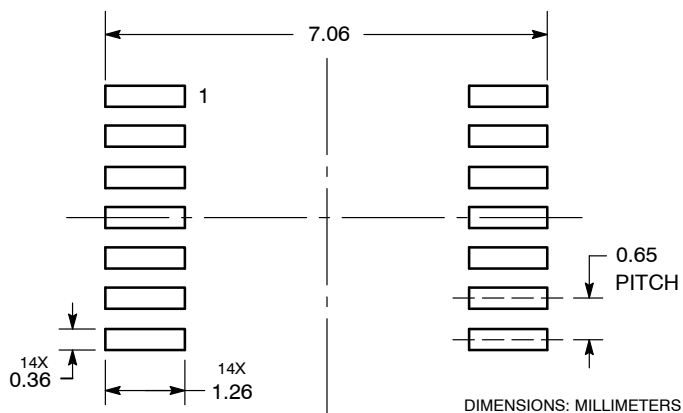
DOCUMENT NUMBER:	98ASH70246A		
DESCRIPTION:	TSSOP−14 WB		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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